Dependable optically differential reconfigurable gate array

Masato Seo and Minoru Watanabe
Electrical and Electronic Engineering
Shizuoka University
3-5-1 Johoku, Hamamatsu, Shizuoka 432-8561, Japan
Email: tmwatan@ipc.shizuoka.ac.jp

***Abstract*—Currently, demand for highly-dependable field programmable gate arrays (FPGAs) is increasing for space systems. However, current SRAM-based FPGAs are vulnerable to high-energy charged particles. Therefore, recently, one type of optical FPGA, optically-reconfigurable gate arrays (ORGAs), have been developed. The reconfiguration of ORGAs is extremely robust because it uses holographic memory technology. However, its robust configuration capability can be increased even further if the number of bright bits or binary state Highs can be decreased by modifying the configuration context pattern. Therefore, this paper presents a dependable optically differential reconfigurable gate array (ODRGA). The experimental results clarify the high configuration reliability of this dependable ODRGA.**

I. Introduction

Currently, demand for highly dependable field-programmable gate arrays (FPGAs) is increasing for use in space systems to realize hardware update and hardware repair functions [1][2][3]. However, current SRAM-based FPGAs are vulnerable to high-energy charged particles in space environments because the configuration context is stored on configuration memory or SRAM. A circuit on a programmable gate array is constantly being damaged. Of course, the use of error checking and correction (ECC) and a scrubbing technique is a useful means to repair it [4][5][6]. However, that technique is incapable of repairing a multi-event upset. Currently, a radiation-error-free programmable device is sought that can be used under such a radiation-rich space environment.

Therefore, a particularly useful type of optical FPGA, an optically reconfigurable gate array (ORGA), has been developed recently [7]-[10]. The function of a programmable gate array of ORGAs is fundamentally identical to that of FPGAs. However, an ORGA includes numerous photodiodes for each programming point of a programmable gate array so that the configuration context can be received optically. An ORGA consists of a holographic memory, a laser array, and an optically reconfigurable gate array VLSI, as shown in Fig. 1. In the device, numerous reconfiguration contexts can be stored on a holographic memory and can be programmed dynamically onto a programmable gate array through a large-bandwidth optical connection between the holographic memory and a programmable gate array. Such high-speed dynamic reconfiguration can increase the performance of a programmable gate array.

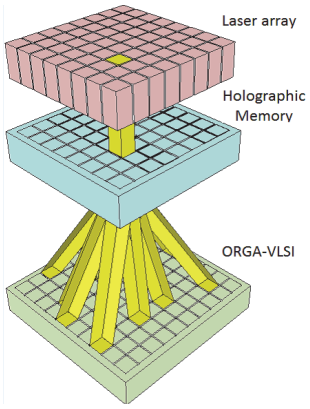

Fig. 1. Overview of an ORGA.

In addition, ORGA reconfiguration is extremely robust because it uses holographic memory technology [11][12]. The holographic memory is well known for its high fault tolerance. Even if a holographic memory and/or holographic memory data is damaged, correct data can be read out. The mechanism of summation of light waves can be regarded as a majority voting operation. Moreover, even if a programmable gate array on an ORGA is temporarily damaged by radiation, the gate array can be repaired in nanosecond order. Therefore, although a programmable gate array part is as sensitive to radiation as a current field programmable gate array (FPGA) is, the gate array's soft-error tolerant of ORGAs can be regarded as very high. Therefore, the ORGA's configuration is actually extremely robust.

However, the robust configuration capability can be increased even more if the number of bright bits or binary state Highs can be decreased by modifying the configuration context pattern. Therefore, this paper presents a dependable optically differential reconfigurable gate array (ODRGA). The experimental results clarify the high configuration reliability of this dependable ODRGA.

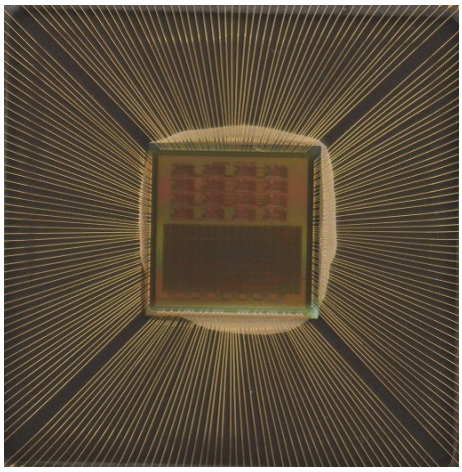

Fig. 2. Photograph of a 0.18 μm CMOS process optically differential reconfigurable gate array VLSI.

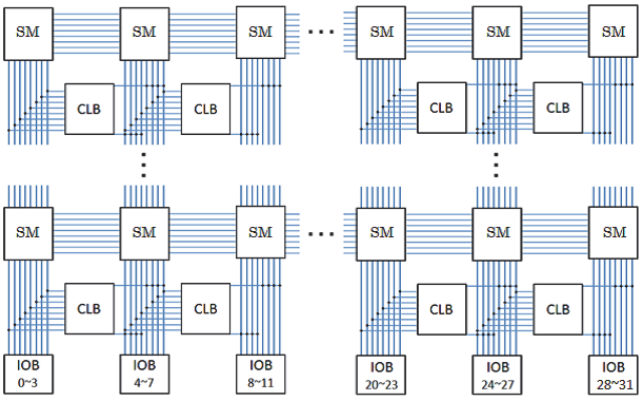

Fig. 3. Block diagram of a gate array.

TABLE I
SPECIFICATIONS OF THE OPTICALLY DIFFERENTIAL RECONFIGURABLE GATE ARRAY VLSI.

Technology	0.18 μm double-poly 5-metal CMOS process
Chip size	5.0 × 2.5 [mm]
Supply Voltage	Core 1.8V, I/O 3.3V
Photodiode size	4.40 × 4.45 [μm]
Photodiode response time	< 5 ns
Sensitivity	2.12 × 10^{-14} J
Distance between Photodiodes	h.=30.08, v.= 30.24 [μm]
Number of Photodiodes	10,322
Number of Logic Blocks	80
Number of Switching Matrices	90
Number of Wires in a Routing Channel	8
Number of I/O blocks	8 (32 bit)
Gate Count	2,720

II. OPTICALLY DIFFERENTIAL RECONFIGURABLE GATE ARRAY

An optically differential reconfigurable gate array VLSI (ODRGA-VLSI) chip was designed and fabricated using a 0.18 μm standard complementary metal oxide semiconductor (CMOS) process technology, as portrayed in Fig. 2. The gate array of the ODRGA-VLSI uses an island style. The basic functionality of a gate array is fundamentally identical to that of currently available field programmable gate arrays (FPGAs) as shown in Figs. 3, 4, and 5. In all, 80 optically reconfigurable logic blocks (ORLBs), 90 optically reconfigurable switching matrices (ORSMs), and 8 optically reconfigurable I/O blocks (ORIOBs), which include 4 programmable I/O bits, were implemented in the gate array. The ORLBs, ORSMs, and ORIOBs are programmable bit-by-bit respectively through 69, 49, and 49 optical connections. The total gate count is 2,720.

A transmission gate and a photodiode cell were designed as custom cells having height equal to that of a standard cell. The gate array design was synthesized by combining such custom cells and standard cells and by using a logic synthesis tool (Design Compiler; Synopsys Inc.). Then, a place and route for the synthesized gate array design was executed using Astro (Synopsys Inc.). Finally, the ODRGA-VLSI was fabricated at Rohm's manufacturing facility. The specifications are presented in Table 1. Voltages of the core and I/O cells were designed, respectively, using 1.8 V and 3.3 V. Photodiodes were constructed between an N-well and a P-substrate. The junction area of a photodiode was designed as 4.40 μm × 4.45 μm. The photodiode cells are arranged at 30.08 μm horizontal intervals and at 30.24 μm vertical intervals. This design incorporates 10,322 photodiodes. To increase the photodiode sensitivity, the photodiode's parasitic capacitance has been decreased. In addition, to realize a differential reconfiguration scheme, toggle flip flops have been implemented behind the photodiodes. The toggle flip flop works as follows. If light is incident to a photodiode, then the connected toggle flip-flop flips its state while light is not incident to a photodiode, the connected toggle flip-flop maintains its current state. Therefore, in the ODRGA, a difference between the current configuration context and the next configuration context is programmed optically onto a gate array. However, under a high-speed dynamic reconfiguration, logic blocks are frequently reconfigured while I/O blocks and switching matrices are rarely reconfigured. Consequently, since configuration is always limited to a look-up table, the differential reconfiguration scheme is very useful to decrease the number of bright bits. Results show that the number of bright bits or binary state Highs can be decreased drastically using this method.

III. EXPERIMENTAL SYSTEM

A. Optical system setup

As depicted in Fig. 6, an ORGA system was constructed using a liquid crystal spatial light modulator (LC-SLM) as a holographic memory and a 532 nm, 300 mW laser. The laser beam was expanded and was used as a collimated beam. In ODRGA, although many lasers must be implemented, we have constructed only a single configuration context ODRGA. Therefore, the single configuration context was implemented onto LC-SLM. The LC-SLM is a projection TV panel (Seiko

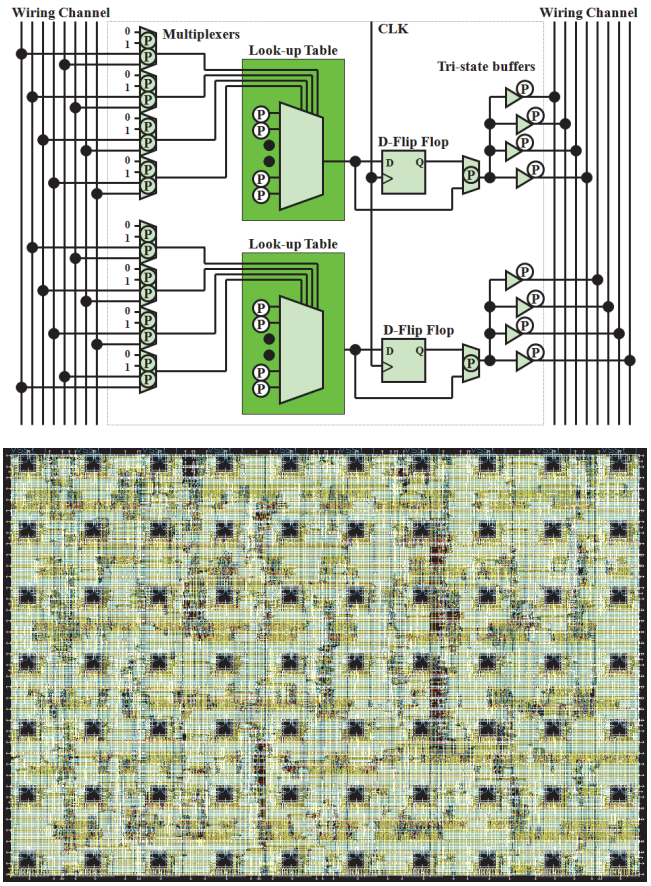

Fig. 4. Block diagram and CAD layout of an optically reconfigurable logic block (ORLB).

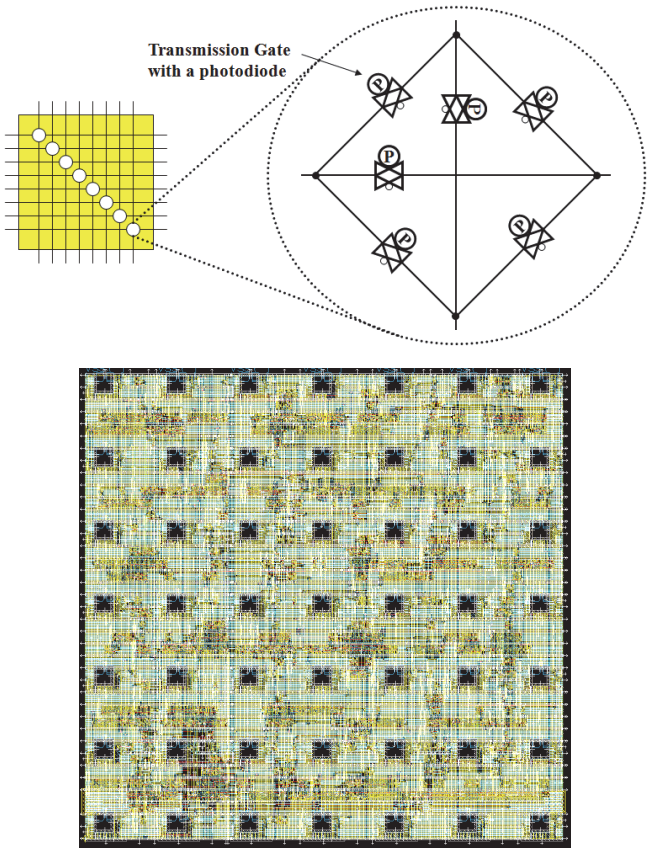

Fig. 5. Block diagram and CAD layout of an optically reconfigurable switching matrix (ORSM).

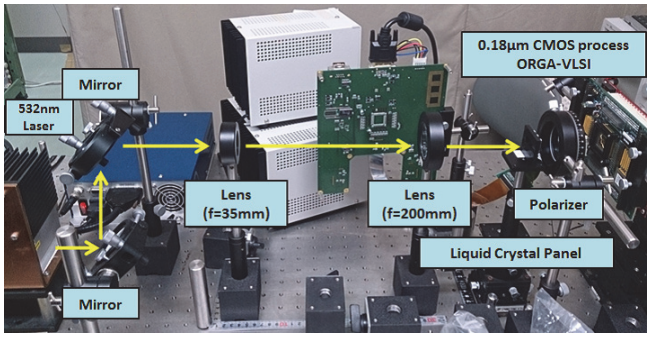

Fig. 6. Optical system.

Epson Corp.), which is a 90° twisted nematic device with a thin film transistor. The panel has 1,920 × 1,080 pixels, each of 8.5 × 8.5 μm^2 size. Among those 1,920 × 1,080 pixels, only 280 × 280 pixels were used as a holographic memory region. The LC-SLM is controlled by a personal computer. The ODRGA-VLSI was placed 80 mm distant from the LC-SLM. The ORGA's control signals were generated using a Cyclone II FPGA (Altera Corp.). All signals were measured using a logic analyzer (16903; Agilent Technologies Inc.).

B. Calculation method of a holographic memory

Here, a thin holographic medium is introduced. An aperture plane of target lasers, a holographic plane, and an ODRGA-VLSI plane are parallelized. The laser beam is assumed as a collimated beam, from which the reference wave propagates into the holographic plane. The holographic medium comprises rectangular pixels of $\delta_x \times \delta_y$ on the $x_1 - y_1$ holographic plane. The pixels are assumed as analog values. The input object comprises rectangular pixels of $d_x \times d_y$ on the $x_2 - y_2$ object plane. The pixels can be modulated to be either on or off. The intensity distribution of a holographic medium is calculable using the following equation.

$$H(x_1,y_1) \quad \propto \quad \int_{-\infty}^{\infty}\int_{-\infty}^{\infty} O(x_2,y_2)\sin(kr)\,dx_2 dy_2,$$

$$r \quad = \quad \sqrt{Z_L^2 + (x_1 - x_2)^2 + (y_1 - y_2)^2}$$

In that equation, $O(x_2,y_2)$ stands for a binary value of a reconfiguration context, k signifies the wave number, and Z_L denotes the distance between the holographic plane and the object plane. The value $H(x_1,y_1)$ is normalized as 0–1 for the minimum intensity H_{min} and maximum intensity H_{max}, as explained in the following.

$$H'(x_1,y_1) = \frac{H(x_1,y_1) - H_{min}}{H_{max} - H_{min}}. \qquad (1)$$

Finally, the normalized image H' is used for implementing a holographic memory. Other areas on the holographic plane are

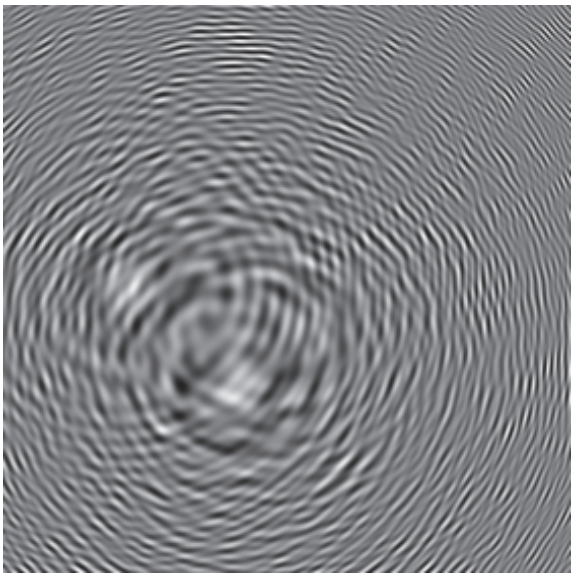

Fig. 7. Holographic memory pattern for a 2-bit adder.

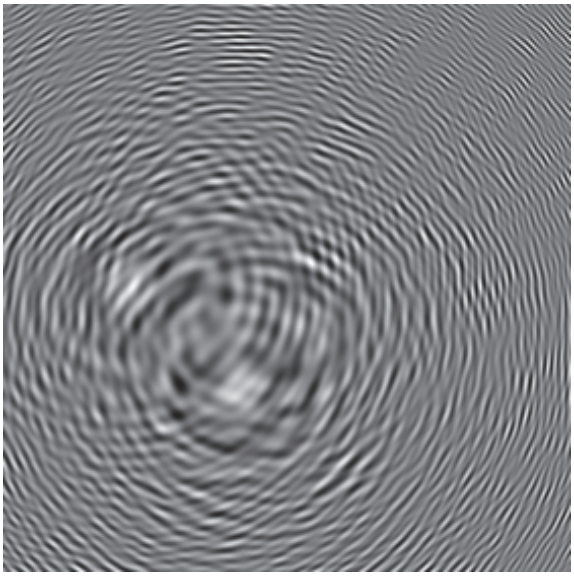

Fig. 8. Holographic memory pattern for a 2-bit subtractor.

opaque to the illumination.

IV. Experimental Results

Using the experimental system explained above, the differential reconfiguration scheme was demonstrated. First, a 2-bit adder and a 2-bit subtractor were implemented for the holographic memory. The holographic memory patterns of the 2-bit adder and the 2-bit subtractor are shown respectively in Figs. 7 and 8. The corresponding CCD-captured configuration context patterns are portrayed respectively in Figs. 10 and 11. These are a normal reconfiguration results.

Then, the differential reconfiguration scheme was confirmed. Here, a situation is assumed in which a 2-bit adder

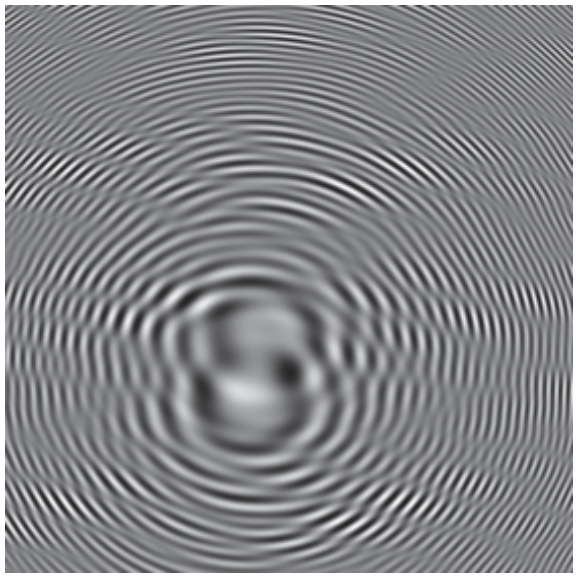

Fig. 9. Holographic memory pattern using a differential reconfiguration.

Fig. 10. Context pattern of the 2-bit adder.

circuit has already been implemented onto an ODRGA. Next, a 2-bit subtractor is being implemented. In this case, the number of bright bits was decreased drastically. The holographic memory pattern of differential reconfiguration scheme from a 2-bit adder to a 2-bit subtractor is shown in Fig. 9. In addition, the configuration context pattern is presented in 12.

Subsequently, impulse noise was applied for the holographic memory patterns of a differential reconfiguration scheme and the 2-bit subtractor. The impulse–noise applied holographic memory patterns are shown in Figs. 13 and 14. Although the impulse–noise ratio of configuration success of the 2-bit subtractor is limited to 20 %, the impulse–noise ratio of configuration success of the differential reconfiguration scheme is as high as 80 %. Therefore, the differential reconfiguration scheme has a drastically higher radiation acceptance ratio.

Fig. 11. Context pattern for the 2-bit subtractor.

Fig. 12. Context pattern of the differential reconfiguration.

V. Conclusion

Currently, demand is increasing for a highly dependable field programmable gate array (FPGA) for use in space systems. However, current SRAM-based FPGAs are vulnerable to high-energy charged particles. Therefore, a type of optical FPGA was developed recently to resolve that problem: optically reconfigurable gate arrays (ORGAs). The ORGA reconfiguration is extremely robust because it uses holographic memory technology. This paper has presented a dependable optically differential reconfigurable gate array. In its architecture, even if 62,720 radiation incidents occur on a holographic memory, simultaneously, a correct configuration procedure can be executed. That fact clarifies its superior high radiation tolerance.

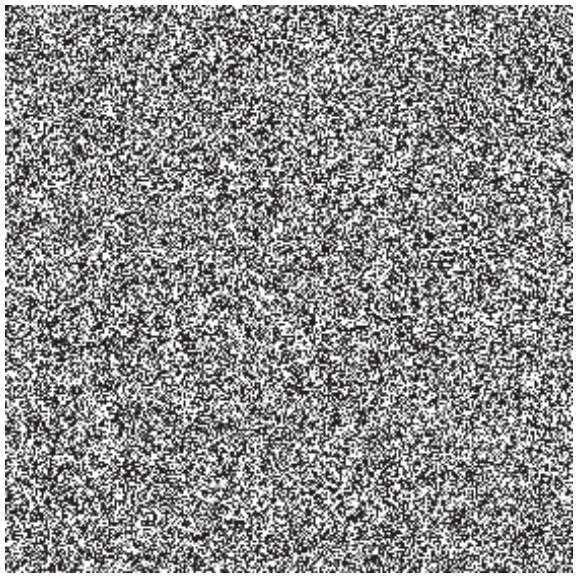

Fig. 13. Hologram of the difference reconfiguration. For 80 % of the hologram area, impulse noises were applied.

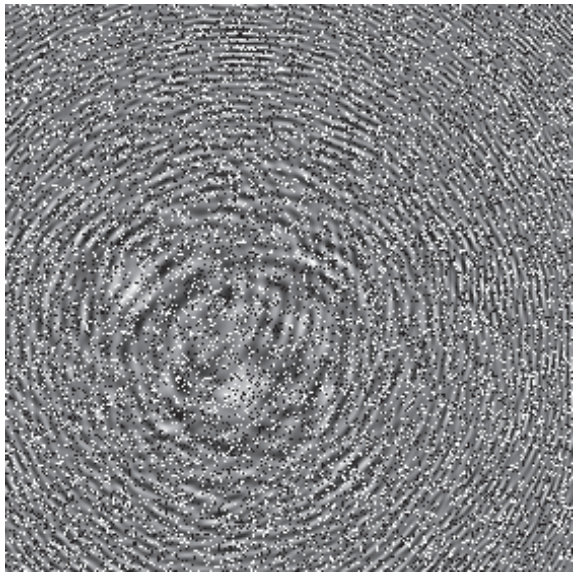

Fig. 14. Hologram of a 2-bit subtractor. For 20 % of the hologram area, impulse noises were applied.

Acknowledgments

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Fig. 15. Context pattern of difference reconfiguration using the holographic memory of Fig. 13.

Fig. 16. Context pattern for a 2-bit subtractor generated from the holographic memory shown in Fig. 14.

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