# K5/VSSP and K5/VSSP32 Data Format

#### update history

2008.07.27 Add a table of sampled data format in a 32-bit word

**2007.10.20** Positions of items (format # and filter frequency) in a aux field were wrong (switched). It was corrected.

### 1 File Structure

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Figure 1: File structure of K5/VSSP or K5/VSSP32 data file. A frame consists of a header block and a data block which contains 1 sec sampled data. Time label of the first sampl in a data block is written in a headder block.

## 2 Header Format

Table 1: K5/VSSP Header Format (64 bits).

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00	sync pattern (all 0xFF)															
0x01	1	sync pattern (an oarr)														
0x02		seconds from 0h UTC (17 bits) (LSB)														
0x03		2n	d syn	ıc pat	tern	(0x8I	3)		AD	bits	san	ıplin	g fre	quency	ch	(M)

Table 2: Typical K5/VSSP32 Header Format (#1) (256 bits).

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00							cune	pattern	( al	1 0vF1	E.)					
0x01							sync	pattern	( aı	1 OXI	L' )					
0x02					sec	onds	from (	Oh UTC	(17	bits)						(LSB)
0x03	2nd	sync	patte	$\operatorname{rn}(0)$	x8C)	(0x8)	B for	VSSP)	AD	bits	san	nplin	g fre	quency	ch	(M)
0x04	eflg   year (2 digits) (6bits: 0-63)   total day (9bits)															
0x05	major version #   minor version #   AUX FIELD size (in bytes : default is 2															is 20)
0x06	LPF frequency (MHz: 0 means through) AUX FIELD format $\#$ (1)															
0x07	station ID (max 2 charcters)															
0x08																
0x09	station name (max 8 characters)															
0x0A																
0x0B																
0x0C																
0x0D						PC	host .	name (n	nav 8	Char	actor	e)				
0x0E						10	11056	name (n	пах С	omar	acter	0)				
0x0F									1 •			•				

eflg: set when error occurred in a previous frame

## 3 Sampled Data Format

Table 3: Sampled data format in a 32-bit word

bit position		31	30	29	28	27	26	25	24	23	22	21	20	19	18	317	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1ch x 1bit	oit sample#		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
1ch x 2bit	sample#	1	6	1	5	1.	4	1	3	12		11		1	10		9	8	3		7	6	3	Ę	0.	4		3		2		,	1
1ch x 4bit sample#			8	3		7				6				5				4	4			(	3		2				1				
1ch x 8bit sample#						4				3				3	3						2	2				,				1			
4ch x 1bit	ch#	4 3		2 1		4 3 2 1		1	4 3 2 1			4	3	2	1	4 3 2 1			4 3 2 1			1	4 3 2 1			4 3 2			1				
	sample#		8	3		7			6				5			4				3		3			2			1		1			
4ch x 2bit	ch#	4	1	3	3	2	2	_	1	4		(	3	2	2		1	4	4		3	2	2	_	1	4	4	(	3	2	2	,	1
4CH X ZDIL	sample#				4	4				3				3	3				2			2							,	1			
4ch x 4bit	ch#		2	1		3			2				1			4			3			2			1								
	sample#								2	2												•				1							
4ch x 8bit	ch#		4								3								2								1						
	sample#																	1															

```
1ch×1bit A/D mode
  1st 32bit data
     D0
            (LSB)
                     1st sampled data (1bit)
     D1
                     2nd sampled data (1bit)
     D31
            (MSB)
                     32nd sampled data (1bit)
  2nd 32bit data
     D0
            (LSB)
                     33rd sampled data (1bit)
     D1
                     34th sampled data (1bit)
     D31
           (MSB)
                     64th sampled data (1bit)
1\text{ch} \times 2\text{bit A/D mode}
  1st 32bit data
     D0
                     1st sampled data (2bit LSB)
            (LSB)
     D1
                     1st sampled data (2bit MSB)
     D2
                     2nd sampled data (2bit LSB)
                     2nd sampled data (2bit MSB)
     D3
            (MSB)
                     16th sampled data (2bit MSB)
     D31
  2nd 32bit data
     D0
            (LSB)
                     17th sampled data (2bit LSB)
     D1
                     17th sampled data (2bit MSB)
     D2
                     18th sampled data (2bit LSB)
     D3
                     18th sampled data (2bit MSB)
     D31
            (MSB)
                     32th sampled data (2bit MSB)
1\text{ch} \times 4\text{bit A/D mode}
  1st 32bit data
     D0
            (LSB)
                     1st sampled data (4bit LSB)
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D3
                    1st sampled data (4bit MSB)
     D4
                    2nd sampled data (4bit LSB)
     D7
                    2nd sampled data (4bit MSB)
     D31
                    8th sampled data (4bit MSB)
  2nd 32bit data
                    9th sampled data (4bit LSB)
     D0
           (LSB)
     D31
                    16th sampled data (4bit MSB)
1ch×8bit A/D mode
  1st 32bit data
     D0
           (LSB)
                    1st sampled data (8bit LSB)
     D7
                    1st sampled data (8bit MSB)
     D8
                    2nd sampled data (8bit LSB)
     D15
                    2nd sampled data (8bit MSB)
     D31
                    4th sampled data (8bit MSB)
  2nd 32bit data
     D0
           (LSB)
                    5th sampled data (8bit LSB)
                    8th sampled data (8bit MSB)
     D31
4ch×1bit A/D mode
  1st 32bit data
     D0
           (LSB)
                    ch1 1st sampled data (1bit)
     D1
                    ch2 1st sampled data (1bit)
                    ch3 1st sampled data (1bit)
     D2
     D3
                    ch4 1st sampled data (1bit)
     D4
                    ch1 2nd sampled data (1bit)
     D5
                    ch2 2nd sampled data (1bit)
     D31
           (MSB)
                    ch4 8th sampled data (1bit)
  2nd 32bit data
     D0
           (LSB)
                    ch1 9th sampled data (1bit)
     D1
                    ch2 9th sampled data (1bit)
     D31
           (MSB)
                    ch4 16th sampled data (1bit)
4ch×2bit A/D mode
  1st 32bit data
     D0
           (LSB)
                    ch1 1st sampled data (2bit LSB)
     D1
                    ch1 1st sampled data (2bit MSB)
     D2
                    ch2 1st sampled data (2bit LSB)
     D3
                    ch2 1st sampled data (2bit MSB)
                    ch3 1st sampled data (2bit LSB)
     D4
     D5
                    ch3 1st sampled data (2bit MSB)
     D6
                    ch4 1st sampled data (2bit LSB)
     D7
                    ch4 1st sampled data (2bit MSB)
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D8
                    ch1 2nd sampled data (2bit MSB)
     D31
           (MSB)
                    ch4 4th sampled data (2bit MSB)
  2nd 32bit data
     D0
           (LSB)
                    ch1 5th sampled data (2bit LSB)
     D1
                    ch1 5th sampled data (2bit MSB)
     D2
                    ch2 5th sampled data (2bit LSB)
     D3
                    ch2 5th sampled data (2bit MSB)
     D31
           (MSB)
                    ch4 8th sampled data (2bit MSB)
4ch×4bit A/D mode
  1st 32bit data
           (LSB)
     D0
                    ch1 1st sampled data (4bit LSB)
     D3
                    ch1 1st sampled data (4bit MSB)
     D4
                    ch2 1st sampled data (4bit LSB)
     D7
                    ch2 1st sampled data (4bit MSB)
     D8
                    ch3 1st sampled data (4bit LSB)
     D11
                    ch3 1st sampled data (4bit MSB)
     D12
                    ch4 1st sampled data (4bit LSB)
                    ch4 1st sampled data (4bit MSB)
     D15
     D16
                    ch1 2ndt sampled data (4bit LSB)
                    ch1 2nd sampled data (4bit MSB)
     D19
     D31
                    ch4 2nd sampled data (4bit MSB)
  2nd 32bit data
     D0
           (LSB)
                    ch1 3rd sampled data (4bit LSB)
     D31
                    ch4 4th sampled data (4bit MSB)
4ch×8bit A/D mode
  1st 32bit data
     D0
           (LSB)
                    ch1 1st sampled data (8bit LSB)
     D7
                    ch1 1st sampled data (8bit MSB)
                    ch2 1st sampled data (8bit LSB)
     D8
     D15
                    ch2 1st sampled data (8bit MSB)
                    ch3 1st sampled data (8bit LSB)
     D16
     D23
                    ch3 1st sampled data (8bit MSB)
     D24
                    ch4 1st sampled data (8bit LSB)
     D31
                    ch4 1st sampled data (8bit MSB)
  2nd 32bit data
     D0
                    ch1 2nd sampled data (8bit LSB)
           (LSB)
     D31
                    ch4 2nd sampled data (8bit MSB)
```