Derivation of the Hardware Specs

These notes have been written to provide background information to "*VSI Interconnect Hardware Specifications*". They generally follow the form of the principal document.

Physical Characteristics

Signal Order in the Connector

Pin allocation has previously been influenced by the recent availability of the SN75LVDS386/387/388/389 16 and 8-bit line drivers and receivers. The proposed new ordering in Table 1 takes this even further, such that the 32 bit streams fit exactly into two 16 bit chips and the remaining signals use as much as required of an 8-bit device. Sensibly the D-flop registers which service these line drivers and receivers would also be 16 and 8 bit chips with the same alignment. In fact one result from modelling realistic interfaces is that at 64 and 128MHz such a structure is essential to allow compensation of chip process skews by tweaking internal clock delays. This applies in both transmitter and receiver circuits.

The second issue is removing all "external" signals like xDATA and the unallocated to the end of the connector so they don't get in the way of the mainstream signal lines. (The names xCTRL, xSPC & xSPD anticipate a proposed allocation for these circuits.)

Thirdly the critical CLOCK signal is protected by placing slow or essentially static signals adjacent to it.

Pin Allocation

The previous pin allocation of signal pairs to (1,41), (2,42)... is convenient in that it allows all the interface ICs and traces to be on one side of the board. Unlike the 40 and 50 pin MDRs formerly considered there are no single in-line surface mount connectors available (which well suited this pinout). Instead, connection to the through hole format splits the pairs between the front and back rows. A simple consideration of the topology shows that this will cause greater impedance discontinuity to each balanced line, and greater coupling to neighbouring pairs, than if pairs are allocated adjacent pins on the same side of the connector.

Curiously it is relatively easy to predict the increased impedance (~57Ohms) but the cross-coupling is beyond guesstimation. But we do recall that a similar circumstance arising from the use of the "historical" T568A/B pin allocations in RJ45 connectors has provided a major obstacle in progressing from Cat 5 to Cat 6 horizontal cable systems.

In the absence of contrary evidence, pins have therefore been allocated in Table 1 to adjacent pairs in the same row, vis: (1,2), (3,4) etc. Running 100Ω balanced microstrip transmission lines to these pins however blocks access to the back row, and these have to be connected via the reverse side of the board. The most effective, and compact solution is to put both the line driver and its register also on the underside. This is only a minor manufacturing inconvenience these days (as looking inside a

mobile phone will soon reveal!). Because these chips are "upside down" the (+,-) pairs are assigned (42,41) etc. rather than (41,42).

The remaining 8 lines are allocated 4 up, 4 down, with the desirable result that CLOCK ends up on the relatively sheltered end position.

Electrical Characteristics

The ultimate objective of performance specs is to ensure interconnectablility of transmission, connection and receiving equipment. To be effective they must account for all the phenomena that degrade the signal path and be realistic with respect to the technology available to build them. Rather than tightly constraining every parameter they should involve measurements which relate directly to the ability of the system to operate correctly, and leave maximum freedom for the designer to choose how to meet the overall objective. Over-specification and too much idealism would rapidly inflate costs with no added benefit. Finally, to prevent the obvious exigencies of the highest frequency designs from driving the specifications at the expense of the others, all timing specifications should scale with rated frequency as far as this is sensible.

With these thoughts in mind an initial set of specs has been tested by developing detailed designs for VSI interfaces for 32, 64 and 128MHz using contemporary technology. The desired objective was to achieve "correct by design" status, i.e. given good construction the design is known to work correctly by relying only on the manufacturer's specifications for the individual components. This was achieved at 32MHz but not at 64 or 128MHz where it proved necessary to match wide registers to the line interface chips, and take out the process skews by tweaking the clock phase to each section. Some minor adjustments were subsequently made to the timing specs to make 128MHz interfaces easier without penalising the basic 32MHz designs.

The situation at high clock rates would be considerably eased by the release of line interface chips with integral registers, thereby greatly reducing total skews. Such an obvious move appears likely since LVDS uses conventional CMOS processes. It seems less likely that 32-bit wide chips will become available as industry is clearly intent on developing GigaHertz serialised data links rather than persisting with fast, wide, data formats like VSI.

The essential features of the final specifications can be seen in Figs 1 and 2. Note that these are not representations of one jittery line, but the **aggregate** of all bit streams on the interface. Two features are immediately obvious: the transmitter is not expected to produce ideal output waveforms, and considerable degradation of amplitude and window width is allowed for in the cable.

Receiver

Starting with Figure 2, the receiver input, we note first that it is not the width of the eye pattern that matters but the interval over which it exceeds the prescribed input threshold. This is $\pm$ 100mV as per Standard '644, and the specification is effectively a rectangular window astride the clock edge. Note also that the clock edge is deliberately early in the window. This is to allow differential (internal) delays as part of the deskewing process. (It is easier to adjust the delays on three clock lines than on 35 data lines!) The width of the window makes provision for residual skews in the

line receivers, setup and hold times in the data registers, and finite precision in adjusting the internal clock delays to the nominal position within the window.

Cable

The allowed signal degradation due to the cable is formally the difference between Figure 1 and Figure 2. (Some more practical if less direct specifications are detailed later in the document.) This provides for attenuation, rise time degradation and intersymbol interference (ISI), all characteristics of a less than ideal lowpass filter, plus skew and cross-talk, including timing jitter induced on the clock signal.

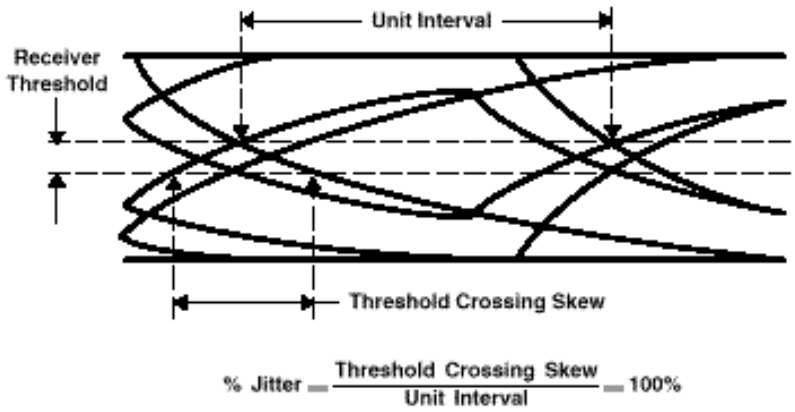

Figure 14. Measuring Signal Transmission Quality

This graphic (from TI document SLLA038.pdf) illustrates the effects of long net rise time on nine or so signal traces. The way low slopes lead to ISI and severe reduction of both the eye pattern width and height, even in the absence of attenuation, is clearly seen. The useful window width, UI-Threshold_Crossing_Skew where UI $\equiv$ T = 1/CLOCK in our terms, is obviously quite sensitive to the size of Receiver Threshold relative to the height of the eye pattern. This diagram shows the situation on a single pair. If equivalent patterns for other pairs are superimposed, with displacements left and right due to pair-pair skews, the valid window width would be reduced much further. It is also clear that if a significant amount of attenuation is added the rise time degradation needs to be greatly reduced or the eye pattern won't cross the receiver thresholds at all, let alone stay open long enough to guarantee correct operation of the receiver hardware.

Skew and rise-time tolerances allowed on the cable obviously subtract from the transmitter and receiver allowances. Most cable performance attributes are linear functions of length and frequency but unfortunately the VSI length specification has oscillated wildly from draft to draft. (One respondent asked for 30m for a DAS-DIM connection, and lengths out to 100m have been mooted, but most figures are in the 15 to 25m range. Our local experience in 9 telescopes and a 7 station correlator is that a mere 4m suffices.) **A maximum length of 20m at 128Msps has therefore been chosen peremptorily**, and the transmitter and receiver timing budgets adjusted to accommodate the performance of the best known cable material, which still takes 30%. It happens that the associated attenuation characteristics match the net amplitude requirements which are already fixed by Standard '644.

Some further words on cable skew and rise times seem to be in order.

Skew ratings range from 500ps/metre for Cat 5E horizontal cable (5E is the up-market cousin of the ubiquitous Cat 5, which doesn't even have a skew rating) down to 35ps/m for Amphenol Skewclear. Since we don't know a priori whether an actual skew will advance or retard a bit stream with respect to its clock, the skew rating subtracts from both ends of the eye pattern. If we therefore allow a total loss of 20% of T to cable skew, then Cat 5E is strictly limited to a mere 6m at 32MHz and proportionately less at higher frequencies. On the other hand the Skewclear comfortably goes 20m at 128MHz.

The effect of cable rise time limitations on signal waveshapes and amplitudes is eloquently illustrated by the familiar diamond-shaped eye pattern. Some examples are 130ps/m for Amphenol Spectra-Coax (a flat ribbon multi-coax) and 36ps/m for 3M's Pleated Foil cable, a similar type of product. Budgeting 10% of T for this effect means that the first type could provide the full 20m at 32MHz but only 12m at 64 and 6m at 128MHz. The 3M cable could provide 20m at 128MHz.

Incidentally it's not that the 3M cable is a super low-loss product, in fact the 90104 series has exactly the same attenuation at 100MHz as the Spectra-Coax. The difference is in the phase characteristics. In fact a cable with higher attenuation can produce a wider eye pattern for digital data. For some pretty illustrations of this try the W.L. Gore website and search for brag sheets on their EYE-OPENER products.

Transmitter

Returning to Figure 1, the 247..454mV amplitude limits are defined by Standard '644. Typical amplitude is 340mV. The drive window is specified at $\pm$ 200mV in anticipation of ~6dB attenuation to the receiver input. Even on a minimum amplitude output the waveform should still be slewing hard at this level to give a crisp measurement. Outside the window 35% of T is allowed for chip skews, timing jitter, rise time and clock position.

A supplementary specification illustrated in Figure 3 constrains waveform slew rates by measuring transition times through the same thresholds as define the drive window. These are easier to measure and more meaningful in our case than the conventional 20%..80% rise and fall times, t_R & t_F, which are dependent on amplitude which in turn may vary over a 2:1 range. Conveniently the two definitions are closely matched for signals which happen to have the nominal 340mV amplitude.

The minimum transition time serves to limit high frequency components (leading to spikes) on the cable. Unfortunately it is simply not practical to specify a scalable value given the range of available hardware. The maximum transition time prevents extreme exploitation of the Figure 1 tolerance for this one parameter, and also provides the only specification on the shape of the rising edge of CLOCK. Unduly slow transition times would render the system more vulnerable to noise.

Timing Budget

Table 2 provides values to all the time specs in Figs. 1 to 3. It turns out that essentially one third of the timing budget is allocated to each of the transmitter, cable assembly and receiver. The actual numbers are fairly "tight" for all three systems at

128MHz (only 7.8ns to do the lot!), but allow progressively more choice of components and circuit design at the lower frequencies.

Times `t3` and `t6` are nominally redundant, but are included because `t1` and `t4` are not easily measurable on some 'scopes. Conformance to **both** `t1` and `t3` will also catch irregularities in the clock period, T, although one would not expect to see any such at a measurable level.

Transmitter Specs (by list item)

1. Basic, defines measurement conditions.
2. Data link Standards (RS-232 etc.) traditionally specify the resting/default state of data lines to the "mark", i.e. "1", state. LVDS receivers are also open-circuit fail safe to the "1" state. Common definition allows systems to be dis/connected and transmitters dis/enabled, without disturbance.
3. It's pointless constraining the cable if unless the transmitter is constrained also.

Cable Specs (by list item)

1. It's not clear that a universal worst-case reference input waveform ensemble exists, and even if it did the complexities of setting up a test generator with 40-odd individual waveforms is likely to be a major exercise in itself.

   Given a "typical" VSI conformant transmitter driving the cable, one could measure its output and carefully scale it according to the actual drive waveforms. To provide better than just a ball-park figure the actual procedure would need to be extensively simulated and carefully specified. This is beyond our present resources.

   In any case some more conventional specifications are needed to select product in the first place. Items 5..7 have therefore been derived empirically to provide a working solution.
2. We had thought to maintain a wider impedance spec to allow designers to take advantage of built-in termination resistors in some line receiver chips. Although these have a nominal resistance of 110Ω the tolerances are so wide (88..132Ω) as to allow excessive reflections on the cable, potentially causing more crosstalk, jitter etc.

   A 10% tolerance is seems generous, but maintaining tight impedance specs on parallel or twisted pair lines is difficult (i.e.expensive).
3. 0.1T of skew closes the data window by 0.2T.
4. Lower rise times close the window at a given amplitude threshold. The effect of a particular rise time is dependent on attenuation.
5. This figure is based on the relative amplitude of the fundamental Fourier component of square and triangular waves approximating the situations in Figs. 1 and 2, plus allowing for the fact that the effective bit rate of CLOCK is twice the data bit rate. The spec is nominally conservative by a dB or so to allow for approximations in the model.
6. In practical cables of any length most crosstalk will occur at the connectors, and then predominantly between near neighbours. However the large number of high speed signals in one interconnect is worrisome, and 7. seeks to limit the total

damage, especially to the critical CLOCK signal.

A swept frequency test is indicated, in recognition of a) the broadband sinx/x spectrum on the data lines, and b) the propensity for resonant effects in long cables with termination defects. Testing much beyond the fifth harmonic is probably not warranted due to the small amount of energy remaining there.

7. See 6.

Receiver Specs (by list item)

1. Even the meanest manufacturer could use 2% resistors to help anchor the total terminating impedance and control reflections.
2. The net terminating impedance at frequency is likely to be complex so a general spec like this is necessary to control reflections on the lines.
3. Most if not all '644 LVDS receivers do so anyway, included in the specifications so designers can rely on it.
4. Note the distinction between signals correctly delivered into a Standard Termination (incident waves) and the actual voltages seen on a receiver connector. The latter may not satisfy Fig 2 due to reflections in that receiver, but the problem is deemed to be 'self inflicted' and the receiver must operate correctly regardless.

Notes on the Specs

Self explanatory.

Measurement Procedures

We note that joining the chasses/grounds together can hide some unwanted effects, hence the caution in item 3. On the other hand ferrite rings should **not** be placed on the VSI cable as suggested at one of our meetings, as they would prevent the cable shielding from doing part of its work.

More Details

A significant amount of detailed information on components and interface design has been accumulated while developing the *Hardware Specs*. Time nor space has allowed its inclusion with these notes. Interested parties may contact the author but there may be some delay in preparing a response.

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