Draft Proposal for VLBI Standard Interface (VSI) Specification

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"Blue Color": Key points, "Red Color" : Comments by H. Kiuchi, CRL on 6 April, 1999

Introduction

The purpose of this document is to define a VLBI Standard Interface (VSI) to and from a VLBI 'Data Transmission System' (DTS) that allows hetergenous DTS's to be interfaced to both data-acquisition and correlator systems with a minimum of effort. The interface is defined to be compatible with traditional recording/playback systems, network data transmission and even direct-connect systems. It is designed to completely hide the detailed characteristics of the DTS and allow the data to be transferred from acquisition to correlator in a transparent manner.

Intent of the Specification

The intent of the VSI specification is to define a standard electrical and timing interface, along with a control philosophy. In this sense, it is not intended to be completely 'plug and play', and will require at least some software customization in each case. Nevertheless, the adoption of a standardized interface at this level should help to relieve many of the existing incompatibilities that now exist between various VLBI data systems.

Assumptions on which VSI specification is based

The following assumptions were made in the development of the VSI specification:

- The DTS is fundamentally a receiver and transmitter of bit streams.
- The meaning of individual bit streams is not specified; normally, a bit-stream will be a stream of sign or magnitude bits associated with particular samples, but the actual meaning is to be mutually agreed upon between the data-acquisition system and the correlator.
- The received and transmitted bit-stream clock rates may be different (e.g. the playback rate of the correlator may be speeded-up or slowed-down), however all bit-stream clock rates on acquisition must be the same, and all bit-stream clock rates on transmit must be the same.
- The data-acquisition time-tag of every bit in every bit-stream must be fully recoverable with no ambiguity.

Discussion

For the purposes of the VSI specification, the DTS is divided into two 'boxes', as indicated in Figure 1:

The 'Data Input Box' (DIB) receives the data-streams and low-level timing information from the data-acquisition system (DAS). Higher-level timing is generated within the DIB itself as will be discussed below.

The 'Data Output Box' (DOB) recreates the data-streams and low-level timing information as an exact replica of that received by the DIB. High-level timing information is managed in a simple interface between the DIB (DOB?) and the correlator such that precisely the correct data are provided at the DIB (DOB?) output.

Operation of the 'Data Input Box' (DIB)

As shown in Figure 1, the DIB has the following interfaces:

1. Interface to the data-acquisition system –
   A number of bit-streams, accompanied by a common CLOCK, and a 1PPS tick which defines the data-bit taken on each second tick (lower-level time tags are specified implicitly as the bit count from the 1PPS tick)
2. Interface to the control computer -
   A control interface used to specify the setting of the Data Observe Time (DOT) clock, and to perform necessary configuration and control functions of the DIB.

The operation of the DIB is as follows:

The DAS is configured as necessary to provide the specified bit streams, along with the accompanying CLOCK and 1PPS tick; the DIB is likewise configured, through its control port, to accept the appropriate number of bit-streams at the specified bit-rate. The 1PPS signal marks the data samples taken on the occurrence of the station second tick (presumably traceable to some station reference clock).

Through the DIB Control interface, the DOT is set to a specified integer second of time (presumably UTC) on a 1PPS tick; the precise method of accomplishing this is not part of the VSI specification. The DOT then keeps time by counting cycles of CLOCK; the data are time-tagged as necessary by the DIB so that each bit in each bit-stream may be recovered with an unambiguous time-tag to the resolution of CLOCK.

The method the DIB uses to record data or to time-tag data is irrelevant to the VSI specification. And, of course, each type of DIB will have various control and configuration requirements which are outside the VSI specification and to which the data-acquisition software must adapt.

Operation of the 'Data Output Box'

As shown in Figure 1, the DOB also has the following interfaces:

1. Output signals to the correlator –
   a) The reconstructed bit streams, accompanied by a common re-constructed clock (RCLOCK) and 1PPS tick (R1PPS). With the exception that these signals may be speeded up or slowed down relative to the rate which they entered the DIB, they are identical reproductions of those entering the DIB.[1]
   b) Each reconstructed bit stream (← Reconstructed bit streams) (RBSn) is (← are) accompanied by a 'common data valid' signal (Vx) which indicates whether the data are believed to be valid or invalid on a bit-by-bit basis.
   c) Time data on ROT must be sent to correlation processor.

2. Input signals and control from the correlator –
   a) A control interface used to specify the setting of the Requested Observe Time (ROT) for Master DOB, and to perform necessary configuration and control functions of the DOB.

[1] Some DIB's (such as Mark III/IV recording systems, periodically replace small portions of the data with synchronization and time code information. In these cases, the DOB must flag such 'replacement data' as invalid.

The ROT maintains the clock and generates a R1PPS ('reconstructed 1PPS') signal to which the reconstructed data must synchronize.

b) A clock from the correlator (← from the Master DOB)(CORRCLOCK) which acts as a reference frequency to the DOB and from which RCLOCK ('reconstructed data clock') is derived. RCLOCK may be at a different rate than CLOCK (corresponding to a speedup or slowdown of the reconstructed data).

c) A CORRTICK signal which sets the ROT clock in a manner similar to the way the 1PPS sets the DOT clock in the DIB. Typically, the CORRTICK signal will be periodic, with a period no shorter than ~1 sec of correlator wall clock time so that a computer control command can be comfortably issued between CORRTICK ticks. Because the correlator is assumed to have some degree of internal data buffering, the CORRTICK signal may be asynchronous with respect to CORRCLK within the limits of this buffering.

Typical operation of the DOB is as follows:

Through its control port, the DOB is configured to reproduce the data streams. The DOB is informed of the number of CLOCK cycles per DOT second so that the DOB knows how many RCLOCK cycles correspond to a R1PPS tick period (and a ROT second). In the case of a recording, tape may have to be positioned to an approximate start-of-scan position.

Through the DOB Control interface, the ROT is set to a specified integer second of time on a CORRTICK tick; the precise method of accomplishing this is not part of the VSI specification. The ROT then keeps time by counting cycles of RCLOCK and generating the corresponding R1PPS signals.

On command, the DOB is responsible for constructing the reproduced bits-streams (RBSx's) properly aligned to ROT, RCLOCK and R1PPS. Since the DOB may not be able to create valid data until after some period of time (due to tape synchronization, etc.), bit streams are individually marked 'invalid' until the DOB is able to provide valid data. Data which are known or believed to be in error (due to tape reading errors, for example) are also marked 'invalid' so that they may be discarded in the correlation processing.[2]

Note that the reconstructed data stream from the DOB is, except possibly for the data rate and for playback errors or intentionally replaced data, identical to the data passed from the DAS to the DIB.

Normally, the CORRTICK pulses would be sent nearly synchronously to all DOB's, causing the DOB outputs all to be time aligned. This is satisfactory as long as the correlator has sufficient internal buffering to adjust the relative the data delays between stations before correlation. If limited internal correlator buffering is available, it may be possible to offset the CORRTICK pulses from one DOB to another to remove the bulk of the desired relative delay. (← relative delay must be controlled inside the DOB, the delay is set by HOST via communication line. So the CORRTICK pulse is 1PPS from the Master DOB.)

The fixed large delay between two stations' data (X- and Y-data) at an epoch on the processing reference time (PRT), is removed by the DOB. The measured phase difference between the replayed and external timing signal sent from the main-DOB-system is monitored by the data clock. The measured data is used for the bit synchronization between the main- and sub-DOB-

[2] In some cases, it may be desirable to inform the DOB of the start and ending times of a scan so that all data outside the scan-time may be marked invalid even though the DOB is reproducing accurate data.

systems. The main-DOB-system and the sub-DOB-systems can be synchronized. The delay adjustment is done inside DOBs.

Since the correlator is presumed to have some internal buffering, R1PPS and RCLOCK need not be precisely aligned with CORRCLOCK and/or CORRTICK; the primary requirement is that the relative timing of R1PPS, RCLOCK and the data/validity lines is properly maintained. (← TBD)

Electrical Specifications

All signals from DAS and to/from correlator are balanced ECL.
Detailed timing specification TBD.
CORRCLOCK frequency – 32 MHz (seems common among systems) (← TBD !!)
RCLOCK frequency – speedup desired when possible.

Physical Connections

DIB: Data, CLOCK, 1PPS – multi-pin connector(s) (TBD)(← D-sub 50 pin)
Control: RS-232(DB-9), GPIB and/or Ethernet (preferred)
Number of bit streams: 2^n (n at least =4) ← 3
Bit-stream data rates: 2^n Mhz (range of n TBD and is system specific)

DOB: Data, validity, RCLOCK, R1PPS , Data synch. Completed, ROT time, etc.
– multi-pin connector (mating to DIB) (← D-sub 50 pin)
CORRCLOCK, CORRTICK, ROT data – TTL 50Ω coax← D-sub 25
Control: RS-232(DB-9), GPIB and/or Ethernet (preferred)

Notes: Input and output connectors and pin-outs should be compatible so that straight-thru cable from DAS to correlator can be used; validity signals should be always be positively asserted in this case.

Control Protocol

Unspecified; system specific.

Questions

What bit-stream rates should be supported?

A DTS should be able to handle individual bit-stream rates of at least 32 Mbits/sec (← 8 Mbits/s), which are easily supported by the specified ECL electrical interfaces. DTS systems for multi-Gb/sec aggregrate rates would be advised to support rates to at least 64 Mbits/sec/bit-stream, and possibly 128 Mbits/sec/bit-stream (← It is difficult on electric cables, but optical fibers.)

How many bit streams should be supported?

This is unspecified, but a maximum realistic number is perhaps 64 (← 32). A 64-bit-stream (← 32-bit-stream) system with 128 (← 64) Mbits/sec/stream would realize an 8 (← 2)Gbit/sec via electric cable, and 16-bit-stream system with 512 Mbits/sec/stream would realize an 8 Gbit/sec via optical cables aggregrate data rate.

Possibility to trade number of bit-streams with bit-stream rate?

System designers are encouraged to design systems which can trade the number of bit-streams with bit-stream-rate, so that the maximum aggregrate rate of the DTS can be utilized as flexibly as possible.

Other notes and comments:

1. Note that the entire DTS can be just a set of straight-thru wires from the DAS to the correlator. In this case, the DOT and ROT are not required since presumably the correlator already is aware of the time. If the data are known to be valid, the validity lines are not needed.
2. For simplicity and flexibility, it is suggested that each input/output data connector carry no more than 8 (← 1) data/validity lines. Each such connector should also carry accompanying CLOCK (RCLOCK) and 1PPS (R1PPS) signals. This would suggest a pin count of 36 signal pins per connector plus some number of additional ground pins. Such an arrangement keeps signals in manageable bundles and allows them to be easily distributed to parallel-architected DTS's. 2*(8data+8valid+clock+1PPS)=36
3. Though there is no specification for allowing dynamic variations in the CORRCLK frequency, some correlator systems could take advantage of a capability that allowed a few-percent (← 0.1*a few %) variation. DTS system designers should specify allowable dynamic variations in the CORRCLK frequency.
4. If the DAS sample rate exceeds the maximum single-bit-stream data-rate, but not the maximum aggregrate DTS rate, the DAS must have the responsibility to do the necessary parallel multiplexing before presentation to the DTS; the correlator, of course, must properly interpret the multiplexed data streams.
5. DOT and ROT should be readable to confirm proper setting.
6. If there is sufficient interest and agreement, a higher-level 'wrapper' specification could be built around this VSI specification; such a specification would include detailed command protocols for controlling the important aspects of the DTS.

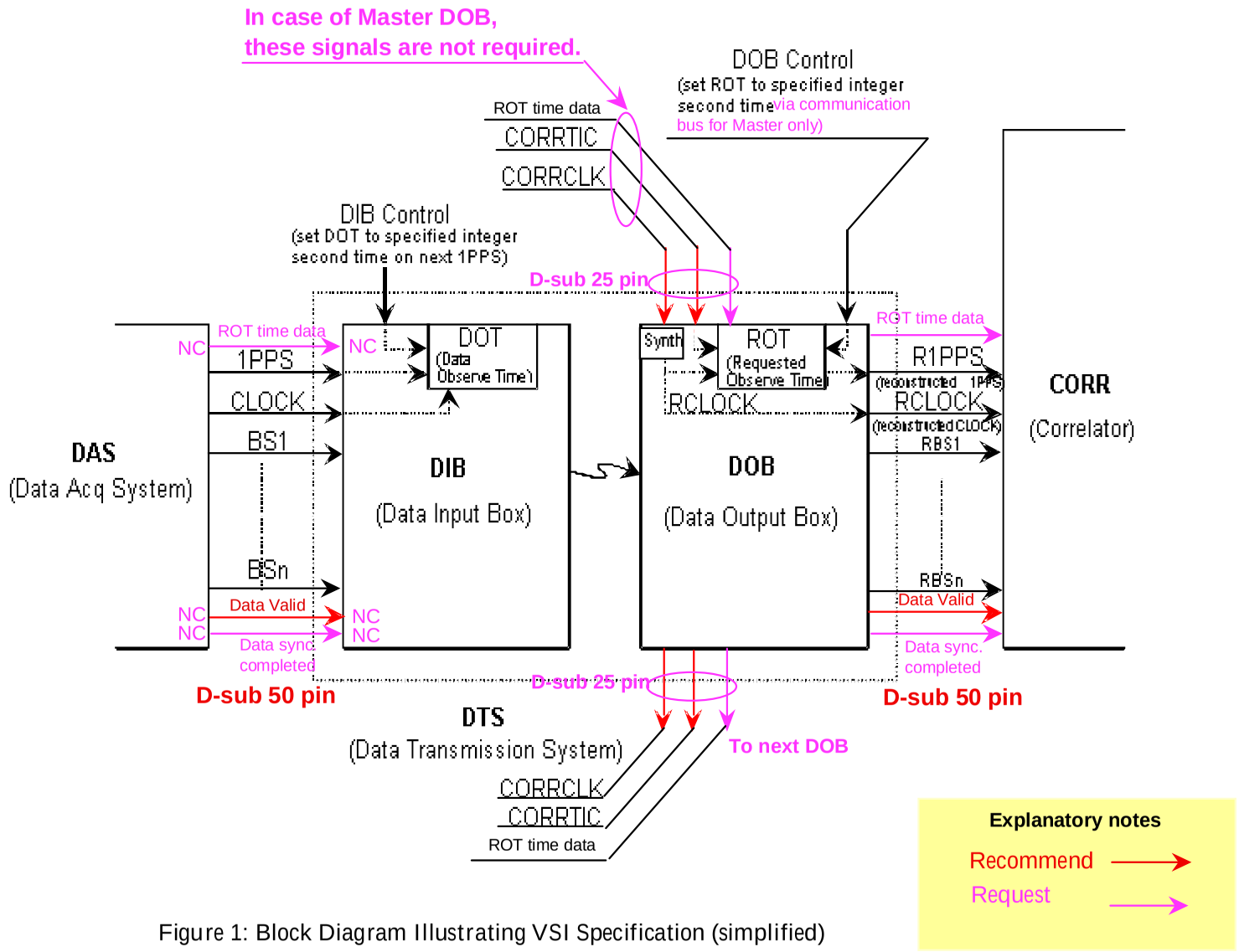

Figure 1: Block Diagram Illustrating VSI Specification (simplified)

D-sub 50 pin connector (female)

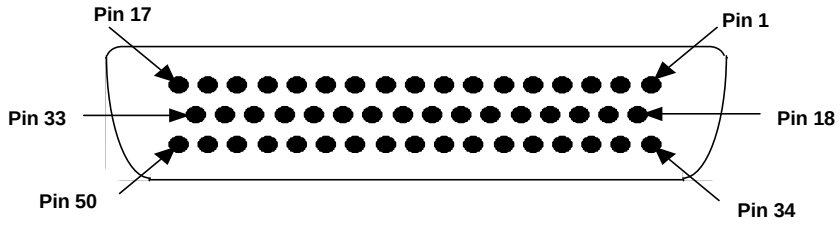

Fig. 2 D-sub 50 pin connector.

Table 1 Pin assign

No.	Name	No.	Name	No.	Name
1	DATA15+	18	DATA15-	34	CLK +
2	DATA14+	19	DATA14-	35	CLK -
3	DATA13+	20	DATA13-	36	Signal GND
4	DATA12+	21	DATA12-	37	1PPS+
5	DATA11+	22	DATA11-	38	1PPS-
6	DATA10+	23	DATA10-	39	Data count H+
7	DATA 9+	24	DATA 9-	40	Data count H-
8	DATA 8+	25	DATA 8-	41	Data count L+
9	DATA 7+	26	DATA 7-	42	Data count L-
10	DATA 6+	27	DATA 6-	43	Reserve
11	DATA 5+	28	DATA 5-	44	Reserve
12	DATA 4+	29	DATA 4-	45	Data Valid+
13	DATA 3+	30	DATA 3-	46	Data Valid-
14	DATA 2+	31	DATA 2-	47	ROT time+
15	DATA 1+	32	DATA 1-	48	ROT time-
16	DATA 0+	33	DATA 0-	49	Parity+
17	Frame GND			50	Parity-

DATA# +/-: DATA No. (ECL balanced data)

CLK +/1: DATA clock (ECL balanced data)

1PPS +/-: 1PPS or reconstructed 1PPS (ECL balanced data)

Data count H +/-: 16 parallel to 32 or 64 parallel (ECL balanced data)

Data count L +/-: 16 parallel to 32 or 64 parallel (ECL balanced data)

Data Valid +/-: Header position marker (ECL balanced data), which is enabled after data synchronization is completed.

ROT time +/-: ROT time (ECL balanced data)

Frame GND: Frame Ground for shield

Signal GND: Signal Ground

Parity +/-: Parity check (ECL balanced data)

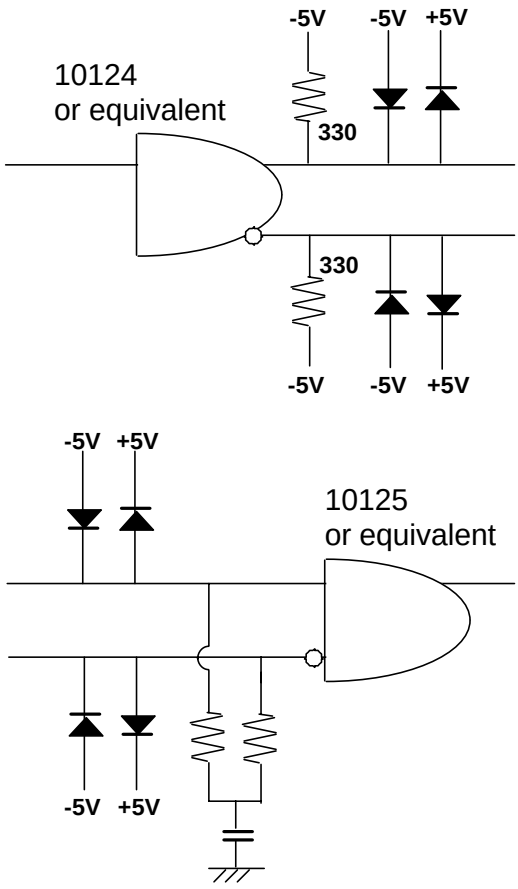

Fig. 3 ECL data transmitter and receiver with protection circuit.