CORRELATION PROCESSING SYSTEM

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Abstract

The new VLBI system is being applied to the Key Stone Project (KSP), which is a metropolitan area crustal deformation measurement project that was started to obtain the precise relative positions of four stations. Three of the four stations are unmanned stations while the central station is manned by one operator who arranges observations and handles correlation processing. There are two different VLBI data transfer modes, one is tape-based and the other is a real-time mode. They have already achieved an accuracy of 1 mm in operation during 24-hour VLBI experiments on alternate days. Since they use the same data interface, the tape-based correlation processing system can be used as a real-time system. We discuss the tape-based correlation. A baseline-correlator has 16 channel units, one unit is a 32-complex-lag correlator with 32-MHz clock. The main component is field programmable gate arrays instead of fully-custom designed ASICs (application-specific ICs). This new correlator enables us to contribute to the geodetic VLBI and also to radio astronomical VLBI.

1. Introduction

We have developed a new correlation processing system. This system was specially designed for the Key Stone Project (KSP), which is concerned with measuring crustal deformation in the Tokyo metropolitan area of Japan. The system was designed to achieve automated operation throughout the entire process; it is operated by one operator who arranges observations and handles correlation processing. The KSP system has two data transfer modes: one is a tape-based mode and the other is a real-time mode. Both modes can be operated simultaneously. In this paper, we discuss the tape-based correlation system. The appearance of the multi-baseline tape-based correlation processing system is shown in Fig. 1. And the real-time

correlation system is also discussed in this special issue.

2. Tape-based correlation processing system

The tape-based (4-station, 6-baseline) system consists of four data recorders, four output interface-units and four digital-mass-storage-systems (automatic tape changers), and six correlation-processors. A block diagram of this multi-baseline system for tape-based VLBI is shown in Fig. 2.

2.1. Data recorder [1]

We used a rotary-head type recorder that uses a cassette tape (American National Standard Institute X3.175-1990 19-mm Type ID-1 Instrumentation Digital Cassette Format). The data recorder's error rates during recording and replaying can be read through a host computer. Helical-scan recording is used to record high-bit-rate digital signals. With a large cassette (16-μm thick tape), the K-4 recorder provides up to 770 Gbits of data-storage capacity. This gives a recording time of 200 min., at a recording rate of 64 Mbps. Recording and playback are possible at different data rates: 256, 128, 64, 32, and 16 Mbps, making the data recorder suitable for many different applications. The playback heads are placed so that the recorded data are immediately played back during recording. This read-after-write facility makes it possible to monitor the recording errors in real time. After correction the bit error rate was better than $1x10^{-10}$. The data recorder has a built-in diagnostic system, which is designed to detect operation errors or hardware faults. Error messages or warning information are fed to the host computer via the remote control interface, and to the front panel display.

2.2. Output-interface

The output interface unit, used at a tape-based correlation processing station, converts the reproduced data into an appropriate output format, and sends them to the correlator. The recorder has helical data tracks: two are longitudinal annotation tracks and one is a control track (Fig. 3). The VLBI data is recorded on the helical data tracks. A set of four helical data tracks has one track set ID number, which is a sequential number used as a tape counter. The track set ID numbers are recorded on the control track, and can be read at any tape speed, even when fast forwarding or rewinding.

The digitized raw data output mode was provided for real-time VLBI via an optical data link. When multi-baseline data are correlated, all the output interface units are daisy-chained via GP-IB and the timing control line. Therefore, the tape position data and the status data of all the data recorders can be exchanged via output-interface units. The main replay system (the main output interface unit and the data recorder) and the sub replay system (the sub output interface unit and the data recorder) can be synchronized in a one-bit step.

2.3. Digital mass storage system (automatic tape changer)

In KSP, we chose an automatic tape changer as a digital mass storage system (DMS). The system accommodates either one data recorder and 24 tapes, or two data recorders and 16 tapes. The maximum mass storage capability is 2.3 TB. A bar-code reader is built into the cassette-handling system to identify individual cassettes within the mass storage system. Information from the bar-code reader is available to the host controller via the remote control interface, and is written on the log which is utilized for correlation processing. Once the observation / correlation tapes have been set in the digital mass storage system, necessary tapes are identified by bar-code labels and are loaded into or unloaded from the data recorder

automatically.

2.4. Data distributor

The data distributor distributes the data from the output interface to the four correlation processors. It can attach a recorder (station) ID to the synchronized data, and the ID is displayed on the correlator front-panel to help identify the processed baseline.

2.5. Correlation processor

The correlation processor was specially designed for the Key-Stone Project. The correlation processing system for the real-time VLBI can use the same correlation system as the tape-based VLBI system. The correlation-processor is an XF type using field-programmable gate arrays (FPGAs) on a VME board. The correlation processor is composed of an input unit, 16 channel units, and a control unit. They are assembled on VME boards. The delay-tracking functions in each unit (channel), which are independent of the frequency, come together in the input unit. One of the 16 channel units is a 32-complex-lag correlator with a 32-MHz clock.

The synchronized signals from output-interface units are fed to the baseline-correlators, which are designed with FPGAs on VMA boards as shown in Fig. 4.

The input unit distributes the data to the 16 channel units. A fixed delay buffer is used for the X data (reference station data), and an elastic buffer is used for the Y data. Delay tracking is done by the elastic buffer. The bit-shift and 90-degree-phase-jump [2] timing are generated simultaneously. The input unit interfaces with the control unit via a VME bus, and interfaces with the correlation units via a VME data bus (user area). Because there are 32 complex lags (32-MHz clock) in each unit, and the correlation processor has 16 channel-units,

the correlation processor is capable of processing data at 512 Mbps and has a total of 512 complex lags.

The counter-fringe rotation resolution is 32 bit; the fringe phase is generated by an equivalent circuit in a modulated numerically controlled oscillator using fractional bit-shift correction. The fringe phase and delay-tracking delay bit can be monitored in real-time. The frequency range of the phase-calibration signal ranges from 10 to 9990 kHz. The correlated results are written onto the NFS-mounted host computer's hard disk via Ethernet.

A priori calculation (Earth rotation parameters: wobble, diurnal polar motion, diurnal rotation, nutation, precession, aberration, time difference, etc.) is done by the built-in control unit.

A fully-custom designed application-specific IC (ASIC) is normally used for high-speed VLBI. However, we use FPGAs instead because they are a kind of reconfigurable ASIC and are suitable for prototyping highly integrated circuits. They are attracting much attention as replacements for customized gate arrays due to their time-to-market advantage and as key devices for future reconfigurable software architectures.

We can debug the correlation algorithms by loading the FPGA configuration data from EPROM, or from a computer via Ethernet, so debugging can be done quickly.

The FPGA configuration is automatically set when booting from ROM or from the host computer (TFTP boot). The FPGA circuit configuration can be changed by downloading a program.

The features of the KSP correlation system are as follows.

(1) It is a multi-baseline system (4 stations with 6 baselines, expandable to 10 stations).

(2) XF-type complex-correlation processing system (32 complex lags/ch x 16 ch in

each correlator).

(3) The maximum data rate is 512 Mbps (32 Mbps (max.) per channel).

(4) Network filing system is supported via Ethernet.

(5) Multi-bit correlation is supported.

(6) Assembled on VME boards.

(7) *A priori* values are calculated in each correlator.

(8) Integration time is 1 to 16 s (1-s steps).

(9) Delay-tracking range is 256 kbit (+/- 128 kbits).

(10) Fringe rotation resolution is 32 bits.

(11) An MC68040 (controller) with a real-time OS is used by the CPU.

(12) FPGA configuration is done automatically via EPROM or an external configuration file (TFTP boot).

(13) The correlation sequence control is automatic (correlation starts when a start time-code is detected in the data and ends when an end time-code is detected).

(14) The correlated results are written in the mass-storage system of the host computer via the Ethernet network filing system.

Since the same data format is used the tape-based correlation processing system can be used as a real-time system.

2.5.1. Built-in input-unit (channel select) of a correlator

As an input-unit, this unit distributes the 16-channel data to correlation units. In this unit, the Y-data is latched by the X-data clock, and the unit generates the timing signals. A fixed delay buffer for X-data and an elastic buffer for Y-data are provided, and the delay tracking is done by the elastic buffer. The bit-shift and 90-degree-phase-jump timings are generated

simultaneously. The input-unit interface with a control-unit is via the VME bus, and the interface with correlation-units is via the VME data bus.

The features of the input-unit are as follows.

(1) X, Y data clock, time-code, data recorder ID detection.

(2) Y-data is re-clocked by X-data clock.

(3) Offset delay control on parameters reference time (PRT).

(4) Delay tracking (+/- 128 kbits)

(5) Supply bit-shift and 90-degree-phase-jump timing to the correlation-unit.

(6) Supply correlation start timing, stop timing to the correlation-unit.

2.5.2. Built-in 16-ch correlation-units of a correlator

A correlation-unit can operate on a 32-MHz clock with 32 complex lags in each unit/channel. The 16 correlation-units has data processing capability of 512 Mbps. The counter-fringe rotation resolution is 32 bits and the fringe phase is generated by an equivalent circuit of the modulated numerically controlled oscillator with a fractional bit shift correction. The fringe phase and delay tracking bits can be monitored in real-time. The frequency of the phase-calibration-signal can be selected from 10 kHz to 9990 kHz. Correlated results are written on the NFS-mounted HOST computer's hard disk via Ethernet.

2.5.3. Built-in a control-unit of a correlator

A priori calculation is done by the built-in control-unit. The following parameters are given by the control-computer via GP-IB.

(1) Frequency table of the channels,

(2) Station positions (X, Y, Z),

(3) Star position (Right ascension, Declination),

(4) ERP (Earth rotation parameters; UT1, X and Y components of wobble),

(5) Correlation start-, stop-time, parameter reference time (PRT),

(6) Video bandwidth,

(7) Directory of the output files of the HOST computer for NFS.

2.6. Control computer

The control-computer controls the DMSs, the data recorders, the output-interfaces, and the baseline-correlators. The control computer gets the following correlation parameters from the host computer via Ethernet: (1) Frequency table, (2) Stations positions, (3) Star position, (4) ERP (Earth rotation parameters), (5) Correlation start-, stop-time, parameter reference time (PRT), (6) Video bandwidth, (7) Directory of the output files of the HOST computer for NFS, (8) Tape ID, (9) Start track-set ID (search for tape start position), (10) Playback data rate. Parameters (1) to (7) are passed through to the baseline-correlators used for a priori calculation and NFS mounting. Parameters (8) to (10) are used for data synchronization. The control computer instructs each DMS to select a tape by its tape-ID, and to mount the tape in the data recorder. The control computer instructs the data recorders to search the start track-set IDs. After that, the control computer instructs the output-interfaces to start data synchronization. It begins automatically. Once it has finished, the correlation process is enabled by the control computer. If the time-on-data is before the correlation start-time, then the baseline-correlator waiting for the time code is detected.

3. Data synchronization sequence

The fixed large delay between two stations' data (X- and Y-data) at an epoch on the processing

reference time (PRT), is removed by the output interface of the tape-based system. The measured phase difference between the replayed and external timing signal sent from the main-replay-system (the main output interface unit and the data recorder) is monitored by the data clock. The measured data is used for the bit synchronization (fine synchronization) between the main- and sub-replay-system (the sub output-interface-unit and the data recorder). The main-replay-system and the sub-replay-system can be synchronized in one-bit steps. The delay adjustment is done by controlling the track-set ID position control and subsequent programmable memory.

The periodicity of the time code is not required for spectrum analysis. Only the sampled data are needed. There is an obvious relationship between the track-set ID (which is a head control signal written on the control track,) and the time code block. It is possible to manage the time code using the track-set ID and time code block. For a few seconds the time code data is overwritten on the data train in a pre-observation header block. After the time code block, data timing is checked by the track-set ID, which means that the output data is only digitized raw data during an observation.

4. Multi-bit correlation

The correlator is basically only a one-bit correlator. However, multi-bit correlation is achieved by input data selection. In the case of the 1-bit (2-level) mode, correlation is done between the same channels of X- and Y-data. In the case of the 2-bit (4-level) mode (Table 1), the MSB data of ch-1 appears in ch-1 and the LSB data of ch-1 appears in ch-2, the MSB and LSB data of ch-2 appear in ch-3 and ch-4, respectably and so on. Then X- and Y-channel selection is as follows.

The line-up of the channel selection of X is ch-1, ch-2, ch-1, ch-2, ch-3, ch-4, ch-3, ch-4, and

so on. That of Y is ch-1, ch-1, ch-2, ch-2, ch-3, ch-3, ch-4, ch-4, and so on. Then, the correlated data of each unit are MSB (ch-1 X) * MSB (ch-1 Y), LSB (ch-1 X) * MSB (ch-1 Y), MSB (ch-1 X) * LSB (ch-1 Y), LSB (ch-1 X) * LSB (ch-1 Y), and so on. After 1-bit correlation, the weight value the correlated results are multiplied by and the sum is calculated by the host computer. So, 16-ch 1-bit (2-level) correlator is equivalent to a 4-ch 2-bit (4-level) correlator. The channel selection is done automatically in 2-bit mode. This scheme is applied to 4-bit (16-level) data.

5. Conclusion

The KSP correlation system was designed to achieve automated operation throughout the entire process; it is operated by one operator for correlation processing. The system has two data transfer modes, one is a tape-based and the other is a real-time. The two systems can be operated simultaneously. The regular geodetic VLBI experiments, every other day 24-hour experiments, have achieved horizontal position uncertainties of about 1 mm [3] and vertical position uncertainties of about 10 mm, in the sense of internal estimation errors evaluated by one sigma standard deviation. All the required processes during observations and data analysis are fully automated, the obtained results are available to the public via the Internet (http://ksp.crl.go.jp). A correlator has 16 channel-units, one unit is a 32-complex-lag correlator with a 32-MHz clock. The main component is FPGAs instead of fully-custom designed ASICs. Using this new correlator, we can contribute to geodetic VLBI and also to radio astronomical VLBI.

References

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[3] Y. Koyama, N. Kurihara, T. Kondo, M. Sekido, Y. Takahashi, H. Kiuchi and K. Heki; “Frequent and Regular Geodetic Very Long Baseline Interferometry Observations with Unattended Observation Control and Data Analysis System”, Earth, Planet and Space.

Fig. 1 Appearance of the multi-baseline tape-based correlation processing system.

On the left side are digital mass-storage systems, and on the right are correlation processor racks. In KSP, there are four sets of digital mass-storage systems, and six baseline-correlators. The output interfaces are at the top, the correlators are the lower two units in each correlation processor rack, and other parts are blank panels. It is possible to extend the system to be 10-baseline correlation system with these three racks. The tapes are loaded into or unloaded from the data recorder (lower side) automatically by the digital mass-storage systems.

Fig. 2 The tape-based correlation processing system.

Fig. 3 Tape format.

Fig. 4 Correlator VME board.

Table 1 Multi-bit correlation mode

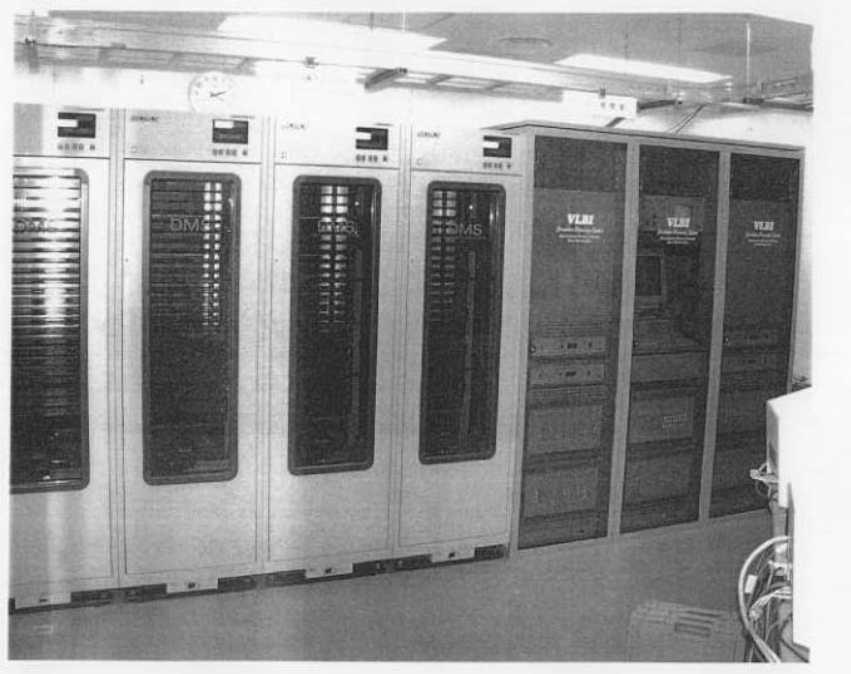

Fig.1

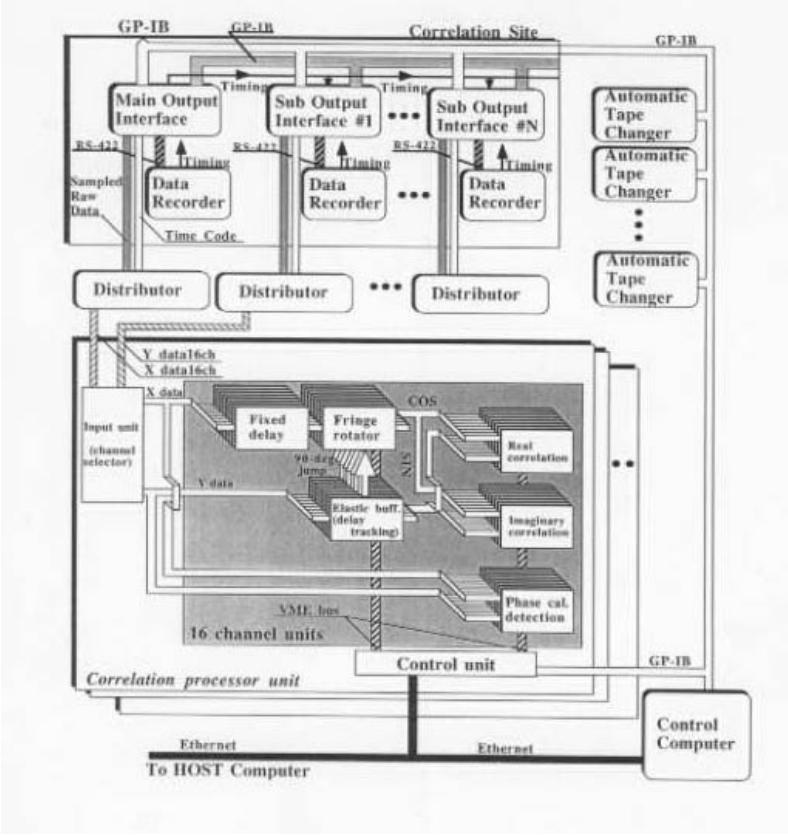
GP-IB
GP-IB
Correlation Site
GP-IB
Timing
Timing
Main Output Interface
Sub Output Interface #1
Sub Output Interface #N
Automatic Tape Changer
Automatic Tape Changer
Automatic Tape Changer
RS-422
RS-422
RS-422
Timing
Timing
Timing
Sampled Raw Data
Data Recorder
Data Recorder
Data Recorder
Time Code
Distributor
Distributor
Distributor
Y data16ch
X data16ch
X data
Input unit (channel selector)
Fixed delay
Fringe rotator
COS
SIN
90-deg. jumps
Real correlation
Y data
Elastic buff. (delay tracking)
Imaginary correlation
Phase cal. detection
VME bus
16 channel units
Control unit
GP-IB
Correlation processor unit
Control Computer
Ethernet
Ethernet
To HOST Computer

Fig.2

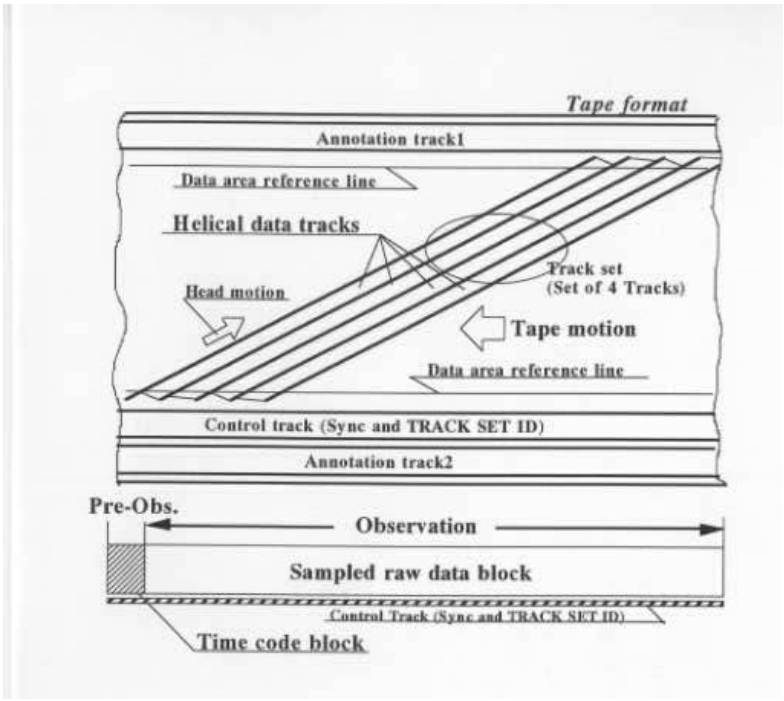
Tape format
Annotation track1
Data area reference line
Helical data tracks
Track set
(Set of 4 Tracks)
Head motion
Tape motion
Data area reference line
Control track (Sync and TRACK SET ID)
Annotation track2
Pre-Obs.
Observation
Sampled raw data block
Control Track (Sync and TRACK SET ID)
Time code block

Fig.3

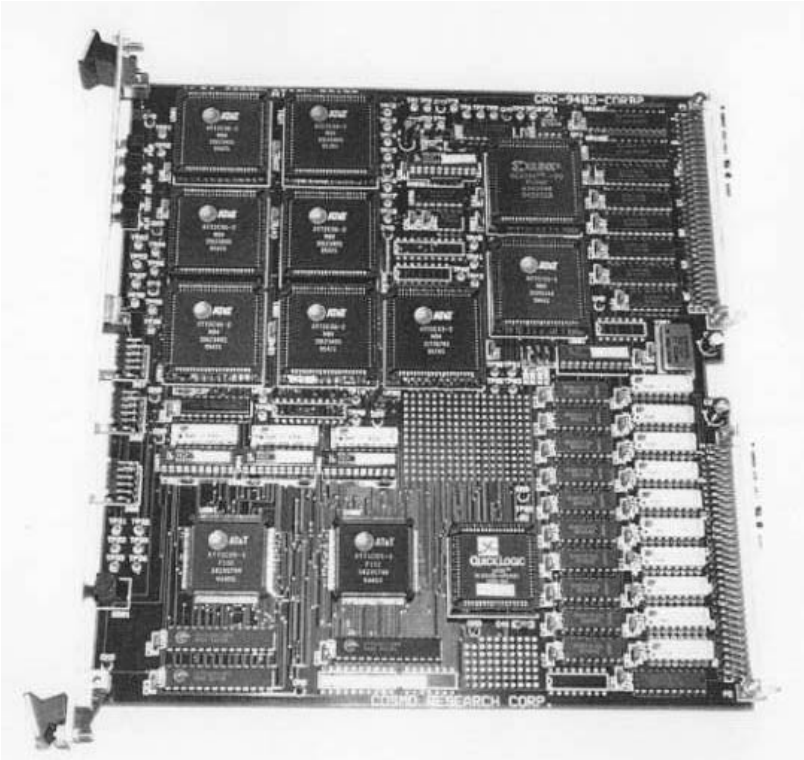

Fig.4

Table 1

1 bit (2 level) Sampling			
channel	A/D conv.	X input	Y input
ch 1	A/D 1	ch 1	ch 1
ch 2	A/D 2	ch 2	ch 2
ch 3	A/D 3	ch 3	ch 3
ch 4	A/D 4	ch 4	ch 4
ch 5	A/D 5	ch 5	ch 5
ch 6	A/D 6	ch 6	ch 6
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
ch 16	A/D 16	ch 16	ch 16

2 bit (4 level) Sampling			
channel	A/D conv.	X input	Y input
ch 1	A/D 1 (MSB)	ch 1	ch 1
ch 2	A/D 1 (LSB)	ch 2	ch 1
ch 3	A/D 2 (MSB)	ch 1	ch 2
ch 4	A/D 2 (LSB)	ch 2	ch 2
ch 5	A/D 3 (MSB)	ch 3	ch 3
ch 6	A/D 3 (LSB)	ch 4	ch 3
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
ch 16	A/D 8 (LSB)	ch 8	ch 8

4 bit (16 level) Sampling			
channel	A/D conv.	X input	Y input
ch 1	A/D 1 (bit4)	ch 1	ch 1
ch 2	A/D 1 (bit3)	ch 2	ch 1
ch 3	A/D 1 (bit2)	ch 3	ch 1
ch 4	A/D 1 (bit1)	ch 4	ch 1
ch 5	A/D 2 (bit4)	ch 1	ch 2
ch 6	A/D 2 (bit3)	ch 2	ch 2
.	.	.	.
.	.	.	.
.	.	.	.
.	.	.	.
ch 16	A/D 4 (bit1)	ch 4	ch 4