



# e-VLBI developments at NICT, Japan

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# Outline

- From K3 to K5
  - a little bit of history
  - Concept of K5 developments
- VSI-E implementation
  - K5 file to Mark5 file transfer over network
- e-VLBI demonstration softwares
- Future plans

# K3 System (1983~1990)



- Purpose : Participation to the International/Global VLBI Observations (CDP, IRIS, ... )
- Objective : Develop an independent VLBI observing/data processing system by maintaining compatibilities with the Mark-III System

# K4 System (1990~1999)



- Objectives : Transportability, Compactness, Automation, High Sensitivity, High Reliability
- Grown to the VSOP system, KSP system, and Gigabit VLBI system

# VLBI Systems : From K3 to K5



K3 Correlator (Center)  
K3 Recorder (Right)

**K3 System**

1983~  
Longitudinal Recorder  
Open Reel Tapes  
Hardware Correlator



K4 Terminal

**K4 (KSP) System**

1990~  
Rotary Head Recorder  
Cassette Tapes  
Hardware Correlator  
e-VLBI with ATM



K4 Correlator



K5 Data Acquisition Terminal

**K5 System**

2002~  
PC based system  
Hard Disks  
Software Correlator  
e-VLBI with IP

# Concept of the K5 System

	K3	K4	K5
Data Recorders	Magnetic Tapes Longitudinal Recorders	Magnetic Tapes Rotary Head Recorders	Hard Disks
e-VLBI	Telephone Line	ATM	IP
Correlators	Hardware	Hardware	Software
	1983~	1990~	2002~
	M96 Recorder, K3 Formatter, K3 VC, K3 Correlator	DIR-1000, -L -M, DFC1100, DFC2100, K4 VC (Type-1, 2), TDS784, ADS1000, GBR1000, GBR2000D, K4 Correlator, KSP Correlators, GICO, GICO2	IP-VLBI (K5/VSSP), PC-VSI (K5/VSI), ADS1000, ADS2000,

# K5 Family : Concept

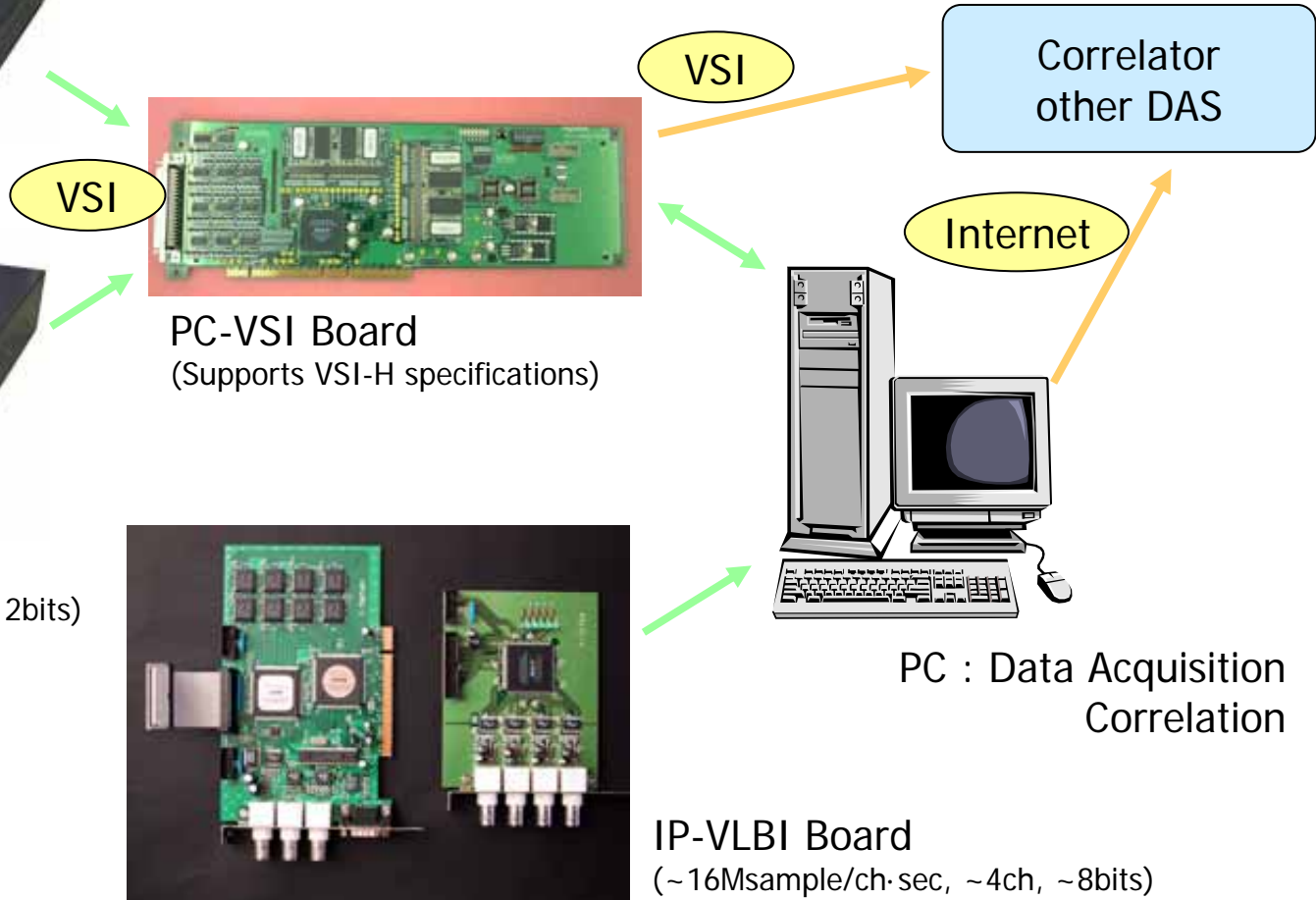
ADS1000

(1024Msample/sec 1ch 1bit or 2bits)



ADS2000

(64Msample/ch·sec, 16ch, 1bit or 2bits)



# K5 Family : Selection of Samplers

	<b>K5/VSSP</b>	<b>ADS1000</b>	<b>ADS2000</b>
Sampling Speed	40, 100, 200, 500kHz, 1, 2, 4, 8, 16MHz,	1024MHz	64MHz
Sampling Bits	1, 2, 4, 8	1, 2	1, 2
No. Channels	1, 4, 16 (with 4PCs)	1	16
Max. Data Rate	512Mbps (with 4PCs)	2048Mbps	2048Mbps



K5/VSSP



ADS1000



ADS2000



# K5/VSSP System

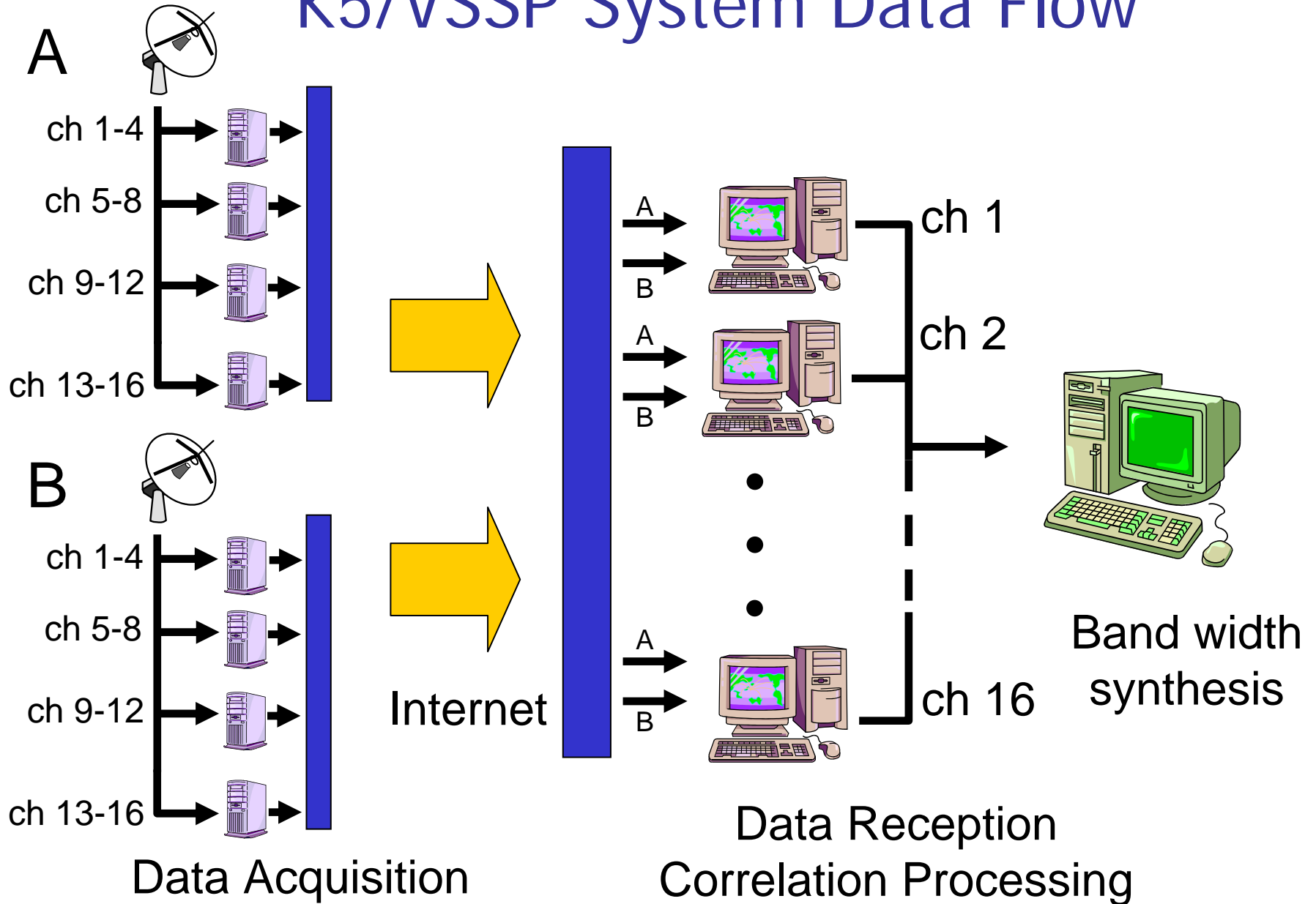
- VSSP = Versatile Scientific Sampling Processor
- 4 Pentium PCs
  - CPU : Pentium-4
    - 1.2GHz (1<sup>st</sup> Unit)
    - 2.4GHz (2<sup>nd</sup> Unit)
  - OS : FreeBSD (Linux is also possible)
  - One K5.VSSP board (PCI) in each PC
  - 120Gbyte HDx4x4 ~ 2.8days@64Mbps
- 16ch base-band signal amplifier
- Standard Signal Distributor
  - 10MHz and 1PPS signals for 4 units



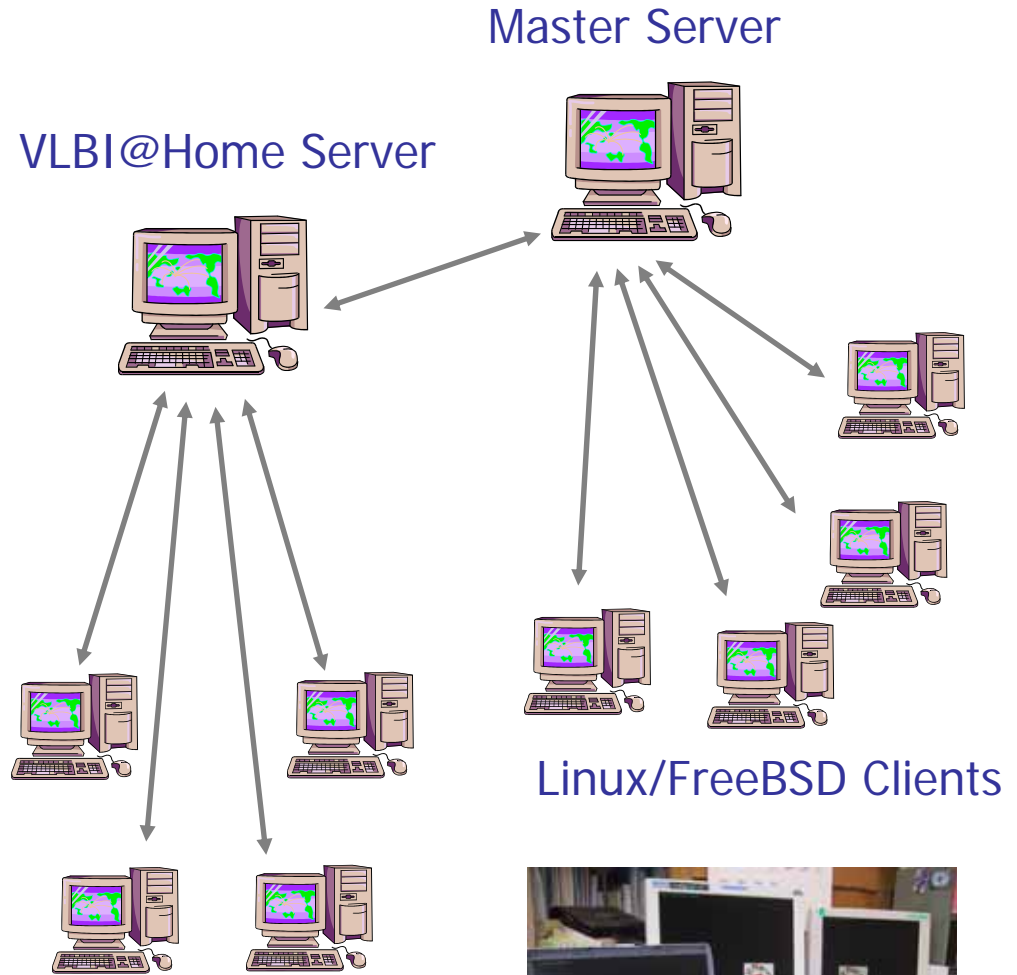
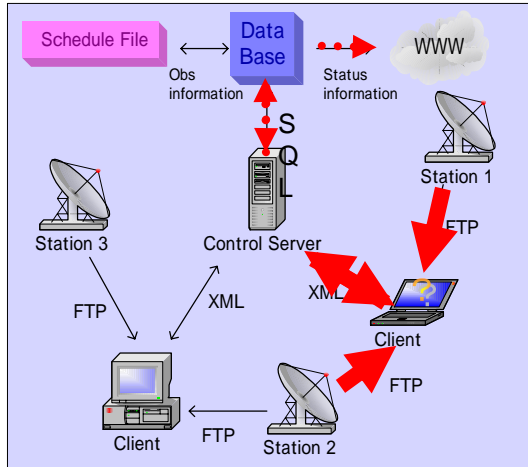
# K5 Systems in use

- IVS stations
    - Kashima (34m, 11m) : NICT
    - Koganei (11m) : NICT
    - Tsukuba (32m) : Geographical Survey Institute
    - Syowa, Antarctica (11m) : NIPR
    - Mizusawa (20m) : NAO/VERA
  - non-IVS stations
    - Peru, Huancayo (34m)
    - many astronomical VLBI stations in Japan
  - Software Correlator Program
    - JIVE, CSIRO/ATNF, e-MERLIN, Viena U. Tech. <sup>\*</sup>,  
CNR/IRA <sup>\*</sup>, KVN <sup>\*</sup>
- \* license agreement in progress

# K5/VSSP System Data Flow



# Distributed Software Correlation



The screenshot shows a web browser displaying a table titled "K.5 相関処理ステータス". The table lists the status of correlation processing for various stations.

観測ステーション	相関処理	相関処理	相関処理	相関処理
観測ステーション	相関処理	相関処理	相関処理	相関処理

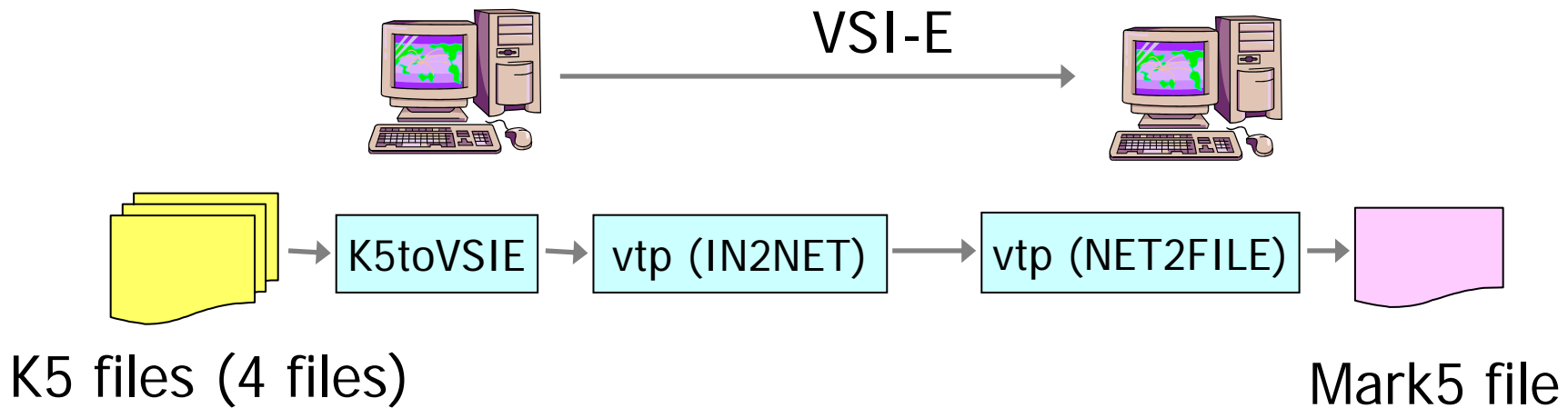
Sta	Position	Appt No.	Match	Appt	Start	Stop
1	ASAC000-001-01	00010100000100	●	00010100000100	00010100000100	00010100000100
2	ASAC000-001-01	00010100000100	●	00010100000100	00010100000100	00010100000100
3	ASAC000-001-01	00010100000100	●	00010100000100	00010100000100	00010100000100
4	ASAC000-001-01	00010100000100	●	00010100000100	00010100000100	00010100000100
5	ASAC000-001-01	00010100000100	●	00010100000100	00010100000100	00010100000100
6	ASAC000-001-01	00010100000100	●	00010100000100	00010100000100	00010100000100
7	ASAC000-001-01	00010100000100	●	00010100000100	00010100000100	00010100000100
8	ASAC000-001-01	00010100000100	●	00010100000100	00010100000100	00010100000100

Correlation Master Table / Database



VLBI@Home Client PCs

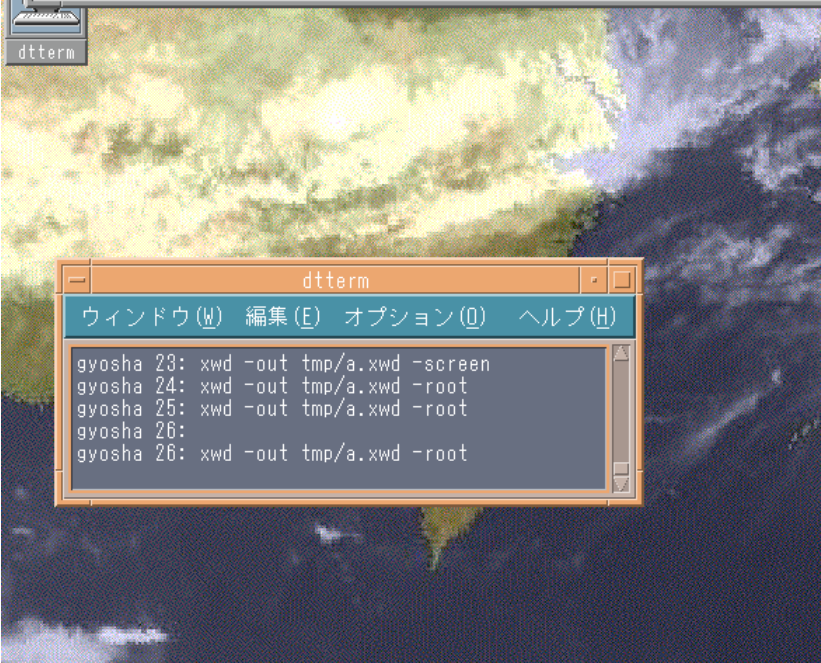
# K5-Mark5 file conversion through VSI-E



\* 'vtp' codes have been developed by David Lapsley and his colleagues at Haystack Observatory

```
dtterm
ウィンドウ(W) 編集(E) オプション(O)
<_ssrc>3</_ssrc>
<_peak_rate>1</_peak_rate>
<_tvq_duration>30</_tvq_duration>
<_protocol>134592789</_protocol>
<_max_time>60</_max_time>
<_rtcp_interval>1</_rtcp_interval>
<_mjd>-1073763048</_mjd>
<_k5udp>-1073763048</_k5udp>
</configuration>
Throughput: 0 bps
Throughput: 6.59995e+07 bps
Throughput: 8.9555e+07 bps
Throughput: 6.31355e+07 bps
Throughput: 2.66525e+07 bps
Throughput: 9.32381e+07 bps
Throughput: 9.32184e+07 bps
Throughput: 7.61851e+07 bps
Throughput: 6.30199e+07 bps
Throughput: 1.82119e+07 bps
Throughput: 9.33392e+07 bps
Throughput: 9.32512e+07 bps
Throughput: 5.85971e+07 bps
Throughput: 8.66659e+07 bps
```

```
dtterm
ウィンドウ(W) 編集(E) オプション(O) ヘルプ(H)
<_ssrc>3</_ssrc>
<_peak_rate>1</_peak_rate>
<_tvq_duration>30</_tvq_duration>
<_protocol>134592789</_protocol>
<_max_time>60</_max_time>
<_rtcp_interval>1</_rtcp_interval>
<_mjd>-1073743528</_mjd>
<_k5udp>-1073743528</_k5udp>
</configuration>
throughput nan
throughput -3.04418e+12
throughput -2.93652e+12
throughput -2.92909e+12
throughput -1.1055e+12
throughput -4.15096e+12
throughput -4.51371e+12
throughput -3.36783e+12
throughput -3.05771e+12
throughput -7.91478e+11
throughput -4.7634e+12
throughput -3.948e+12
throughput -2.70545e+12
throughput -4.3674e+12
```



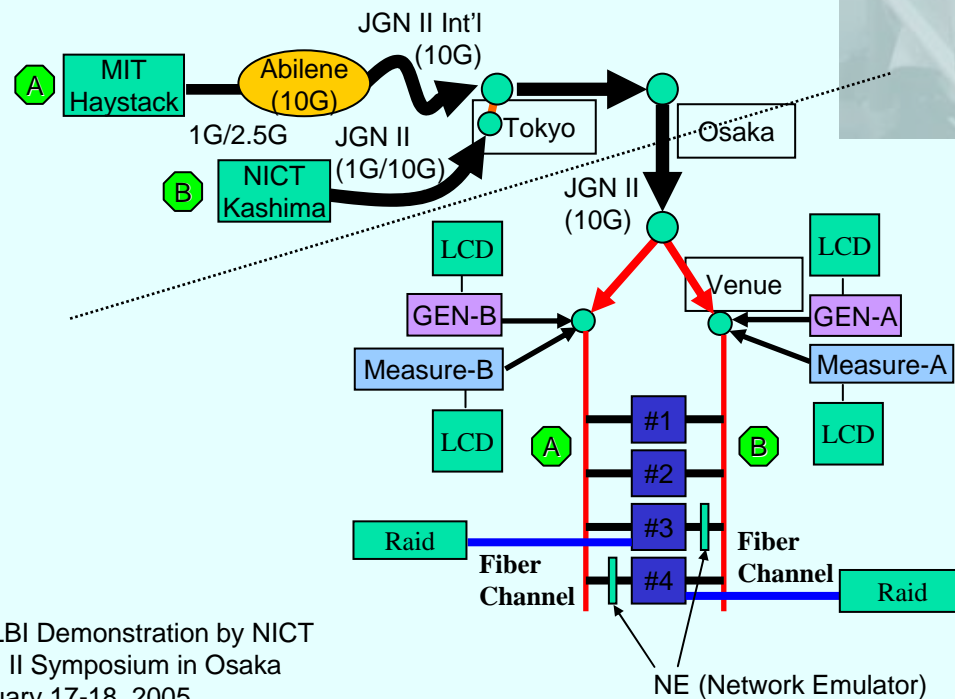
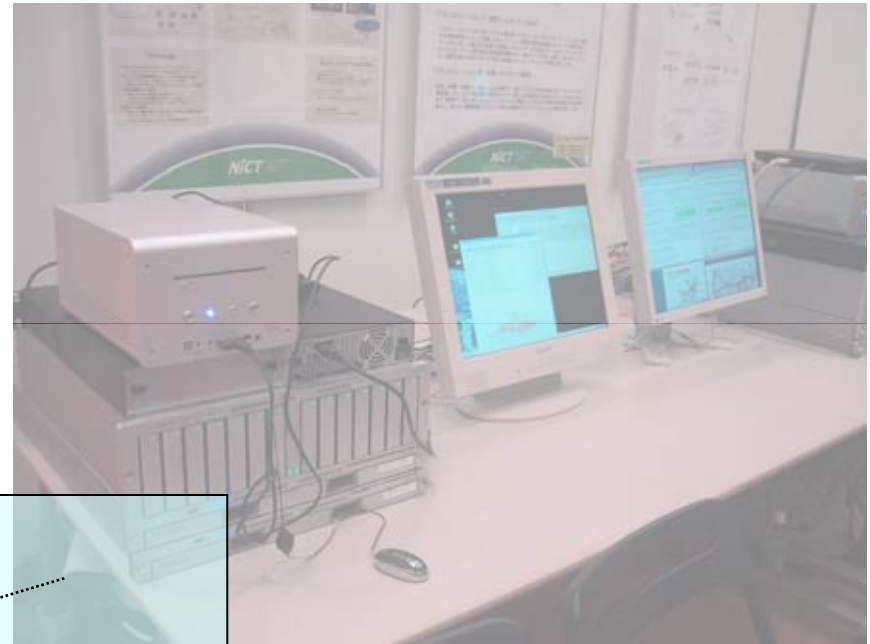
```
dtterm
ウィンドウ(W) 編集(E) オプション(O) ヘルプ(H)
Data read: 2000000
Channels: 4
Quantization: 1 bit(s)
Frequency: 16000000 Hz
Time: 61203 secs after midnight
./run.sh: line 3: 4912 Broken pipe                               /home/vlbi/K5toVSIE/K5toVSIE 535
20 U151170000a.dat U151170000b.dat U151170000c.dat U151170000d.dat 127.0.0.1
vlbi2.jp.apan.net 48: more run.sh
#!/bin/sh
cd /mnt/raid/R1177
/home/vlbi/K5toVSIE/K5toVSIE 53520 U151170000a.dat U151170000b.dat U151170000c
.dat U151170000d.dat 127.0.0.1
vlbi2.jp.apan.net 49: cd /mnt/raid/R1177
vlbi2.jp.apan.net 50: /home/vlbi/K5toVSIE/K5toVSIE 53520 U151170000a.dat U15117
0000b.dat U151170000c.dat U151170000d.dat 127.0.0.1
Data read: 2000000
Channels: 4
Quantization: 1 bit(s)
Frequency: 16000000 Hz
Time: 61201 secs after midnight
```

```
dtterm
ウィンドウ(W) 編集(E) オプション(O) ヘルプ(H)
gyosha 23: xwd -out tmp/a.xwd -screen
gyosha 24: xwd -out tmp/a.xwd -root
gyosha 25: xwd -out tmp/a.xwd -root
gyosha 26:
gyosha 26: xwd -out tmp/a.xwd -root
```

System tray area containing a clock showing 7月 11日, a volume control icon, a network status icon, a printer icon, a mouse icon, a keyboard icon, a help icon, and a power icon. The text '9 IR1' is visible in the bottom right corner.

# Real-time software correlation demo

Real-time software distributed correlation was demonstrated at JGN2 symposium in Osaka (January 17-18, 2005). Fake random data were generated at Kashima and at Haystack and transferred to Osaka by using Abilene and JGN2. The data were correlated by using 8 CPUs (Apple X-serve G5) and about 400Mbps throughput without fringe rotation processing was achieved (the speed was limited by the network data transfer).



e-VLBI Demonstration by NICT  
JGN II Symposium in Osaka  
January 17-18, 2005

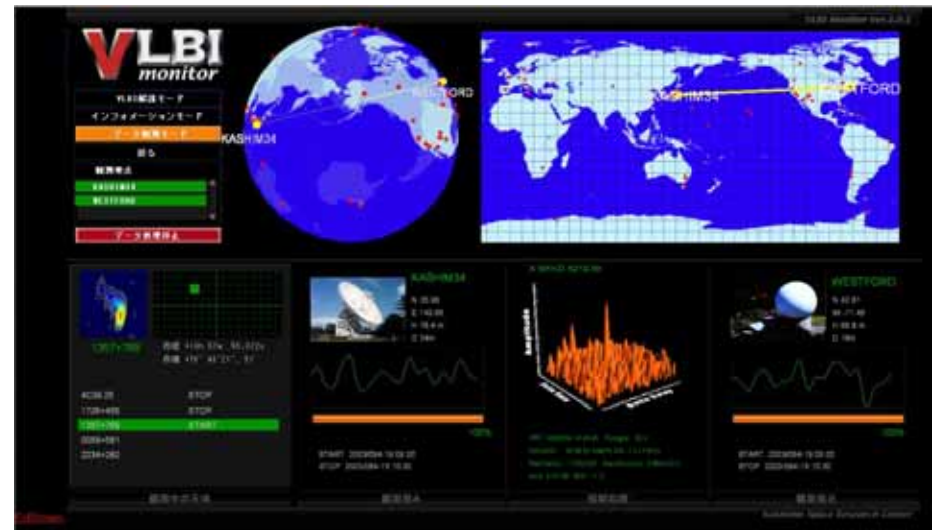
The data were correlated by using 8 CPUs (Apple X-serve G5) and about 400Mbps throughput without fringe rotation processing was achieved (the speed was limited by the network data transfer).

# Another recent event at Kashima

Emperor and Empress of Japan visited Kashima and they learned about e-VLBI (June 5, 2005)



Demonstration software was developed. The software was designed to be useful for actual operation, too.



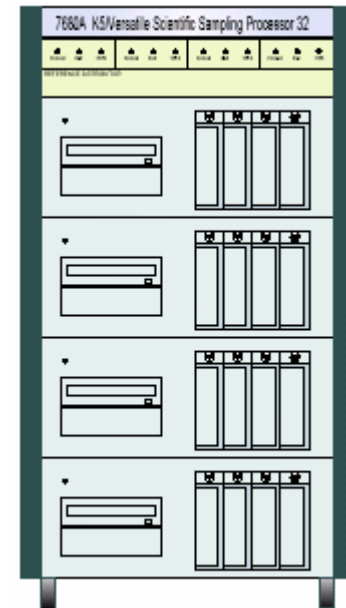


# Future Plans (1)

- K5 Upgrade



Interface	K5/VSSP32	K5/VSSP
Sampling Speed	40kHz ~ 32MHz	40kHz ~ 16MHz
Sampling Bits	1, 2, 4, 8	1, 2, 4, 8
No. Channels	16	16
Max. Data Rate	1024Mbps	512Mbps
Interface to A/D	USB2.0	PCI
Disks	SATA (hot swap)	PATA
OS	Fedora Core	FreeBSD/Red Hat Linux



K5/VSSP32

# Future Plans (2)

- Operational software correlator for VERA and KVN
  - 1Gbps/station (max.) x 5 stations (10 baselines) by using 5 dual CPU PCs in case of VERA
  - Target : Operational by the end of 2006
- Further VSI-E implementation
  - A/D Sampler => VSI-E
  - VSI-E => Software correlator
- Digital BBC
  - Off-line processing : realized – ex. Huygens session
  - Real-time processing : requires FPGA, developments in progress