

CSP (Central Signal Processor)

CSP-MID

VLBI Beam former

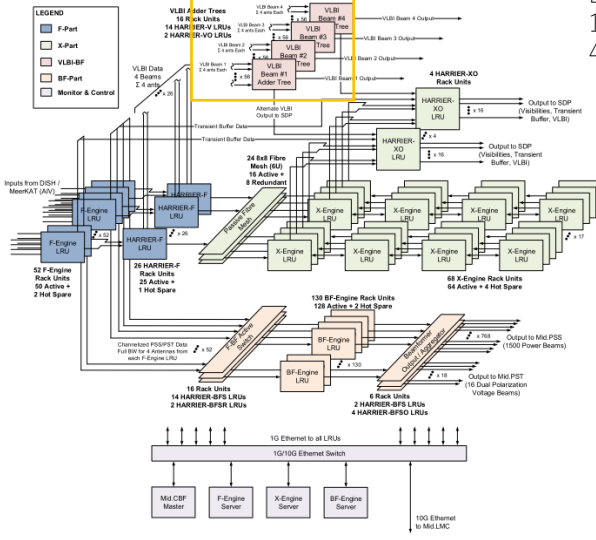
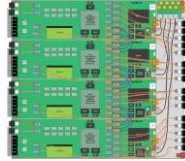


Figure 5-14 Mid.CBF Top Level Physical Architecture

1U / board, total 300 boards
Altera Stratix 10 FPGAs
Liquid cooling
16ラック
400kW power



主な仕様

REQ-366	Within the bandwidth claimed to be spectrally pure, CSP_Mid.CBF shall induce no spectral distortion in the VLBI data above -40dB TBC in amplitude and 1e-2 radians TBC in phase after calibration.	REQ-349	When performing VLBI beamforming, the CSP_Mid.CBF shall achieve a Signal to Noise ratio better than 98% compared to an ideal analogue beamformer, given the same digitized inputs and calibration.
REQ-358	Upon command from CSP_Mid.LMC, CSP_Mid.CBF shall re-configure the centre frequency, frequency band, and/or bandwidth for each tied-array VLBI beam, in less than 20 seconds (TBC).	REQ-353	CSP_Mid.CBF shall be able to output VLBI beams with a sampling rate selectable between Nyquist and at least factor 2 oversampled rates for the selected bandwidth.
REQ-1647	CSP_Mid.CBF shall send tied-array beam data to pulsar search and timing, and VLBI outputs, with a maximum latency of 0.1 seconds (TBC).	REQ-352	CSP_Mid.CBF shall be able to generate data from the VLBI beams with samples traceable to a timestamp with an accuracy of 1 nsec or better.

Table 5-2 The observation bands and other key parameters of SKA1 Mid and MeerKAT.

Band	Frequency Range (GHz)	Bandwidth to be delivered to the SCP (MHz) as visibilities	Sample Word-Length input to Mid.CBF	Common Sample Rate (GSPS) input to Mid.CBF
SKA1 Band 1	0.35 - 1.05	700	8-bit	4
SKA1 Band 2	0.95 - 1.76	810	8-bit	4
SKA1 Band 3	1.65 - 3.05	1400	8-bit	3.2
SKA1 Band 4	2.80 - 5.18	2380	4-bit (TBC)	12
SKA1 Band 5	4.60 - 13.80	2 * 2500	4-bit	2 * 6
MeerKat UHF-Band	0.58 - 1.015	435	TBD	TBD
MeerKat L-Band	0.9 - 1.67	720	10-bit	TBD
MeerKat S-Band	TBD	TBD	TBD	1.712
MeerKat X-Band	TBD	TBD	TBD	TBD

VLBI ビームフォーマー構成

局数：200 (SKA1+MeerKAT)
帯域：Max 80Gbps/局
同時出力ビーム数：4
DBBC Tunable 10kHz
BW: 1, 4, 16, 32, 64, 128, 256, 512 MHz
記録帯域：80Gbps x 4beams

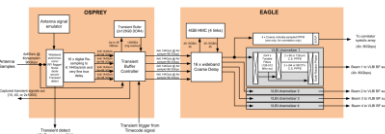
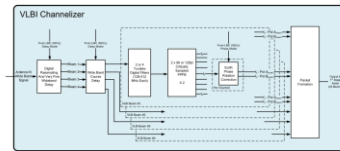
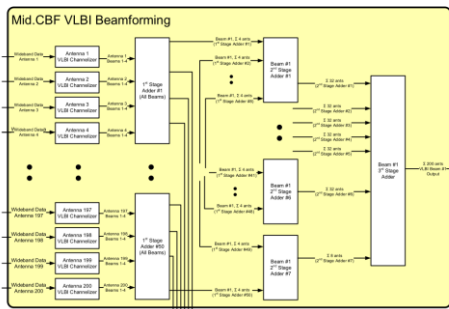


Figure 6-4 Functional allocation of VLBI-mod signal processing in the F-part to the DSPREY and EASLE modules. The flexible VLBI channelizer allows to also re-configure and re-configure further refinement taking into account system requirements and FPGA processing resources. Transient detection and triggering by the same as in Figure 6-3. With associated data paths (not shown) the Transient Buffer Controller could capture data after the established capture delay or even after the VLBI channelizer is in operation.

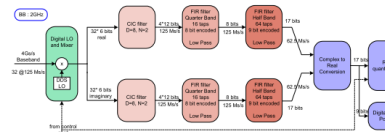


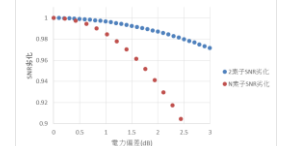
Fig. 3: Electronic architecture of the 3-stage FFB

NAOJ開発

DBBC : OCTAD同等であり着実な開発が可能
REC : OCTADISK2を40GbE化する
スケジュール
2018 概念設計、2019~PM



ビーム合成帯域内振幅特性偏差によるSNRの劣化



SKA2に向けた基礎開発テーマ

1. 分散計算機 + 低消費電力IO

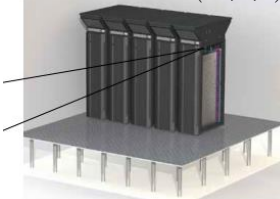
~Post Mooreの計算機技術~

MIDではFIREFLYを採用
1.5W/28Gbps=50mW/Gbps
↓
光IOコア (PETRA) 5mW/Gbps



2. 低消費電力冷却

SKAMID CoolIT(カナダ)



液設計算機
東工大 TSUBAME KFC
KEK SUIREN
RIKEN
<http://www.el.gsic.titech.ac.jp/~endo/publication/endo-hokke13-slides.pdf>

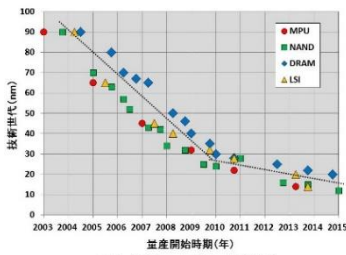


図1 急ブレーキがかかる微細化
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