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III. VLBI SYSTEM

III. 4 K-3 AND K-4 VLBI DATA CORRELATION PROCESSORS

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ABSTRACT

In this paper, the performances of the K-3 correlation processor and the development plan of the K-4 correlation processor are presented, both are developed by the Communications Research Laboratory, Ministry of Posts and Telecommunications, Japan (CRL).

The K-3 correlation processor was developed to interface to the K-3/Mark III data recorder(1) in order to process Japan-US VLBI experiments. The K-3 correlation processor provides high speed processing and a long integration time, and it has been working as the only VLBI correlation processor in Japan. One type of the outputs of the K-4 data recorder's output interface is designed to be compatible with K-3/Mark III data recorder in order to enable processing data by the K-3/Mark III correlation processor(1).

The K-4 correlation processor is completely designed using the advanced functions of the K-4 data recorder, such as a fully synchronization of the data stream. The K-4 correlation processor is targeted as the next-generation processor.

1. Introduction

After being acquired on magnetic tape by a VLBI data acquisition terminal, a large quantity of data should be processed by a correlation processor.

In this paper, the performances of the K-3 correlation processor and the development plan of the K-4 correlation processor are presented.

2. Outline of the K-3 VLBI Correlation Processor

The K-3 correlation processor was completed in 1984 by CRL. A block diagram of the K-3 correlation processing system is shown in Fig. 1. The performances of the K-3 correlation processor are shown in Table 1. The K-3 correlation processor consists of four "crates", and each crate consists of one controller, seven channel units and one reserve unit.

The main performances of the K-3 correlation processor are:

1) Compatibility

The K-3 correlation processor is fully compatible with the Mark III VLBI data format(2), which is commonly used for precise geodetic VLBI experiments.

2) Expandability

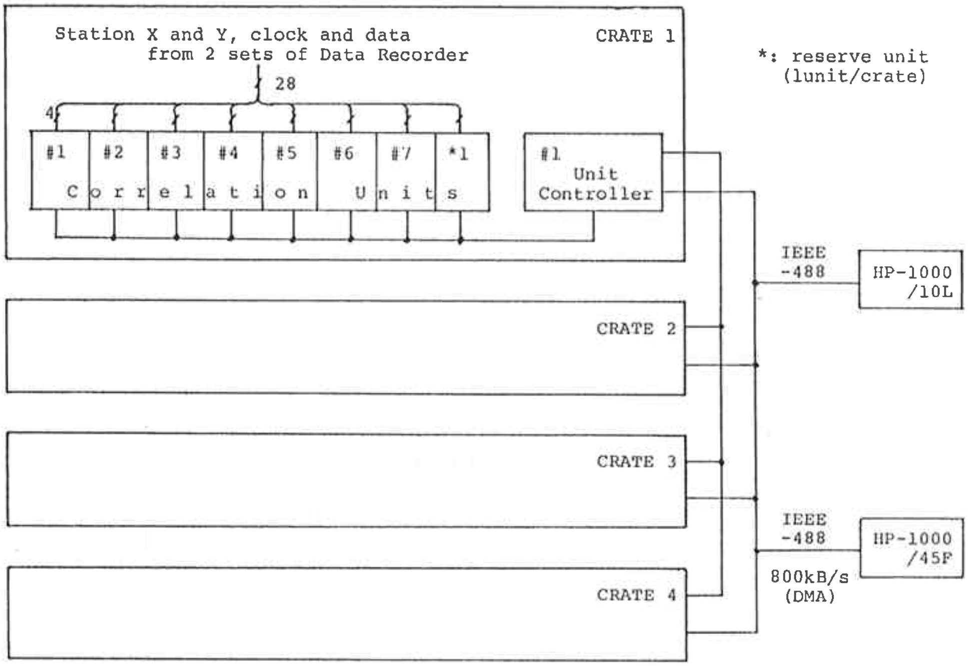


Fig. 1 Block diagram of the K-3 correlation processor.

Table 1 Performances of K-3 correlation processor

structure	8 channels × 4 crates
max. channels	32
max. processing speed	8 Mbps
programmable delay	128 bits
correlation lags	complex 8-bit lags
integration period	5 ms to 8.38 sec at 4 Mbps
buffer memory	20,000 bits
phase calibrator	complex 24 bits
host computer bus	IEEE-488, 800 kbyte/sec
	fringe rotator
phase resolution	0.02 microradian
phase rate resolution	0.93 mHz (selectable)
phase acceleration	capable
fringe pattern	3-level
fractional bit correction	90 deg. jump

Each crate works independently, so more crates can easily be added for multibaseline processing. When an additional data recorder is used, a 4-crate processor can simultaneously process data of two baselines at 14-channel mode.

3) High-speed processing

The K-3 correlation processor can process at any reproduction data rate up to 8 Mbps. This means that reproducing speed can be twice the usual recording speed in order to reduce the data processing time.

4) Long integration time

Delay changes during a long integration time are compensated for by a 128-bit programmable delay circuit. A fringe rotation, caused by the earth's rotation, is compensated by using a sinusoidal function of three-level approximation. The resolution, which is the minimum quantized fringe frequency, is high enough to integrate the correlation data for a long period with a slight loss. Furthermore, fringe acceleration is also compensated for and a fractional bit is corrected. These are made in the time domain in order to simplify the hardware.

These factors make possible a longtime integration of correlated data of up to 8 seconds at a rate of 4 Mbps with low coherence loss (4% by fringe rotation compensation, and 3.4% by fractional bit compensation) at any intercontinental baseline. The raw data are condensed into processed data, the ratio of which is 10 ppm, with a slight loss of the delay information.

5) Real-time checking of correlation unit

The host computer can alternately check seven units during operation by comparing the correlation data from the operation unit with those from the reserve unit. Once the host computer finds a failure unit, it calls the operator and automatically replace the failure unit with the reserve unit. In this way, nonstop processing can be achieved even if one correlation unit in one crate fails.

3. Detailed Description of the K-3 Correlation Processor

The block diagram of one correlation unit of the K-3 correlation processor is shown in Fig. 2. PP (parameter period) is a fundamental period of the correlation processor. The processor integrates the correlated data during the PP using its own hardware. It receives the integration parameters, such as calculated delay rate and fringe rotation, at the beginning of the PP (BOPP) from the host computer. The processor then sends the correlated data to the host computer.

1) Detection of the header and frame synchronization

The observed time should be recognized in the correlation processor in order to make correct correlations. The header is recorded in each frame (20,000 bits), and includes the synchronization pattern and observed time code. The Mark III format shown in Fig. 3 has no error correction. Therefore, the bit error rate (BER) is approximately 10^{-4}, which is much worse than in case of digital communication. For VLBI data processing, a BER of 10^{-4} only deceases the correlation amplitude by 0.01%. However, when a high BER causes a wrong time code during reproduction, a serious synchronization error happens.

The reproduced data and clocks of station X and station Y are input into the decoder. The decoder reproduces the data Xd and Yd" using the clock, and it makes the frame synchronization using the time codes.

The header has a CRC (cyclic redundancy check) code in order to detect the bit error. When the decoder detects the CRC error, it sets the TWE (time word error) status in order to inform the analysis computer.

The clock is derived from the reproduced data. The addition or omission of the clock can happen when the BER is extremely high. In that case, the correlation is made using the wrong time. The decoder detects

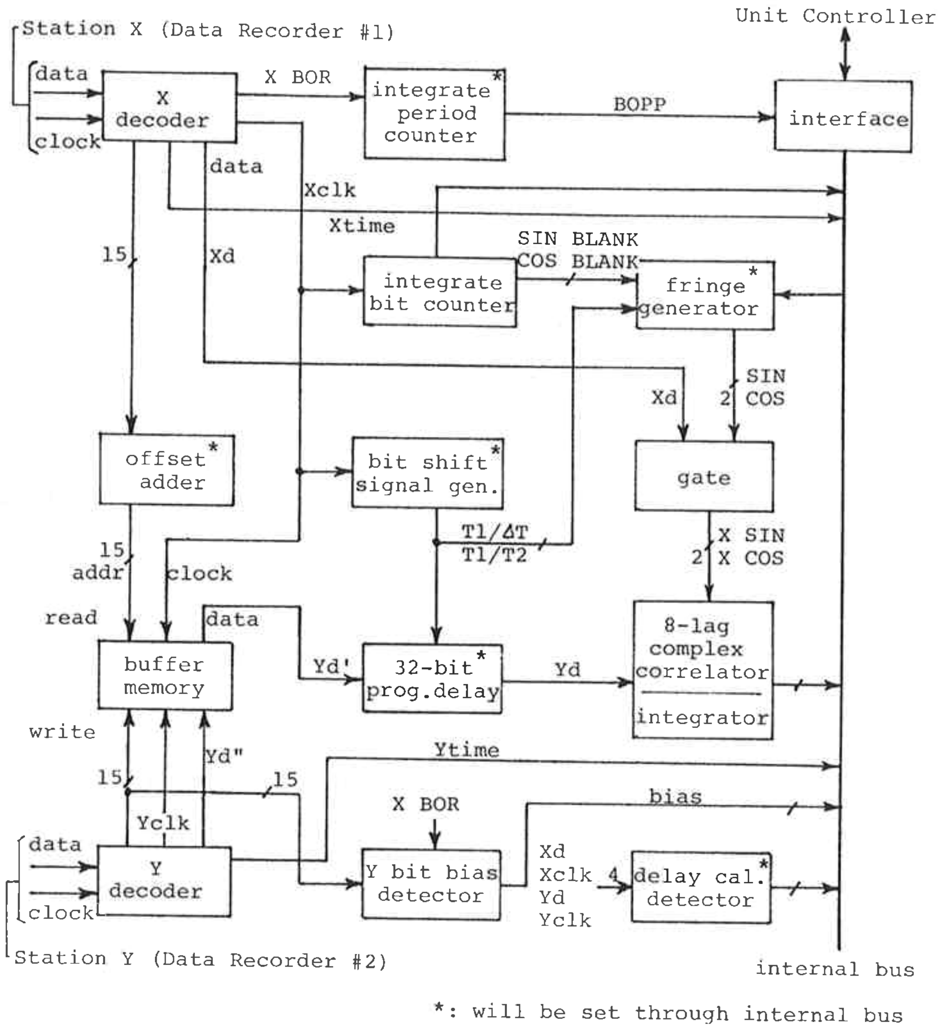


Fig. 2 Block diagram of the correlation unit of the K-3 correlation processor.

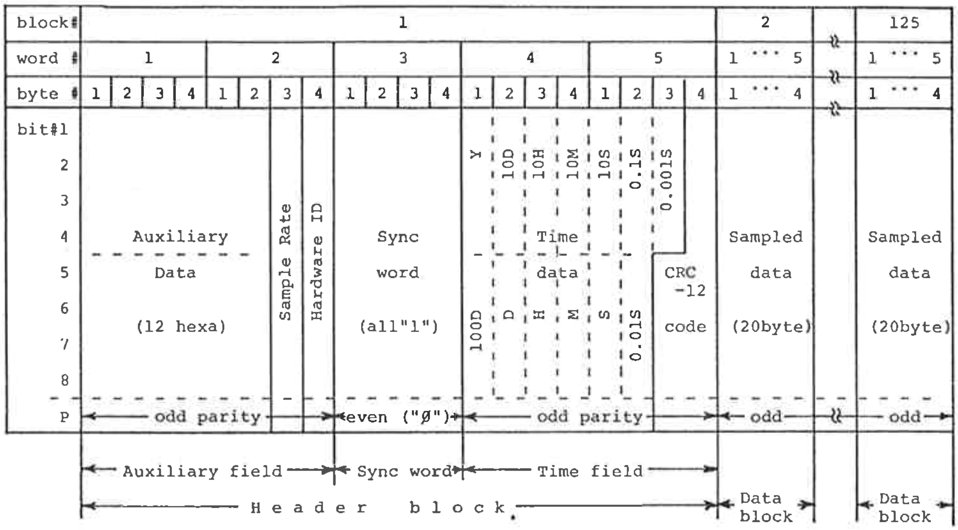
this error by comparing the clock number between the frame synchronization pattern. The error resets the correlation available flag, which lets the host computer know if the correlated data can be used.

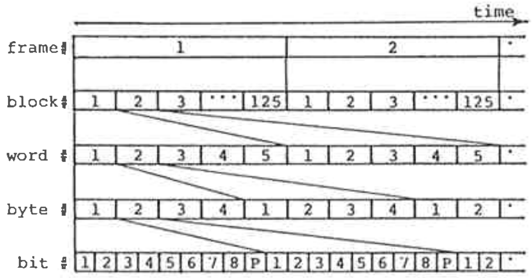
The decoder also measures the BER using the parity bit in order to monitor the quality of the recording and reproduction.

2) Bit synchronization

The reproduced data of the data recorder is not fully synchronized and contains some jitter. Before the correlation, the data of the two stations should be synchronized by removing this jitter.

The station Y data, Yd", whose parity bit is already removed by the decoder, are written onto the buffer memory of 20,000 bits. This is the same number of bits in one frame. The station Y clock, Yclk,





	blocks	words	bytes	sample bits	tape bits
1frame=	125	625	2,500	20,000	22,500
1block=	1	5	20	160	180
1 word=	–	1	4	32	36
1 byte=	–	–	1	8	9

Fig. 3 Mark III VLBI data format.

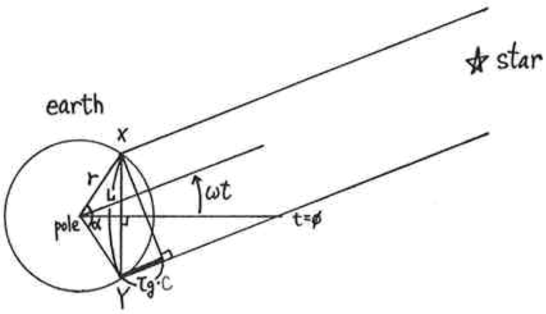


Fig. 4 Schematic diagram of VLBI experiment.

is used when the data are written into the memory, and a value of the bit counter of the decoder Y is used as the memory address. The memory is read at the timing of the Xclk with an address offset set by the host computer. The station Y data, Yd', which are read from the memory are correlated with the station X data, Xd, when the data recorder output difference is within 20,000 bits. This amount equals a tape length of 17 mm.

In this way, perfect synchronization is achieved.

3) Compensation of the delay time

The schematic diagram of the VLBI experiment is shown in Fig. 4. L is called the baseline length which is a distance between two VLBI stations, X and Y. The radio waves from the star can be defined as being parallel, because of the great distance between the earth and stars. The delay time τ_g is the time difference between received time at X and Y, and is written as:

$$\tau_g = L / C \sin \omega t. \quad \cdots\cdots (1)$$

The delay rate τ_g', derived from Eq. (1), is:

$$\tau_g' = (2r / c) \sin a\omega \cos \omega t. \quad \cdots\cdots (2)$$

When X and Y are located on opposite sides of the earth and the star is at the zenith of vector L, the maximum τ_g'max is:

$$\tau_g' \max = 2r / c \cdot \omega = 3.15 \; [\mu s / s]. \quad \cdots\cdots (3)$$

During integration, the maximum number of the bit shift $S_b$max can be calculated as:

$$S_b \max = (\tau_g' \max T) / t_s = 100.8 \; [\text{bit}]. \quad \cdots\cdots (4)$$

Here, the integration period T is 8 seconds (nominal), and the sampling interval t_s is 250 ns (nominal at 4 Mbps).

To compensate for this delay, the K-3 correlation processor has a 128-bit programmable delay circuit, which dynamically tracks the delay during the integration period.

The delay rate also changes during the integration, but the maximum rate is 114 psec/sec/sec[3]. This shows that compensation is not necessary, because the error of only 11 degrees during an 8-second period of integration causes a slight coherence loss, which can be ignored.

4) Compensation of the fringe rotation

The Doppler effect causes the phase rotation during the integration, which is called "fringe rotation". The maximum fringe rotation frequency F_r max is:

$$F_r \max = \tau_g' \max \cdot f = 27.1 \; [\text{kHz}] \quad \cdots\cdots (5)$$

where f is the RF frequency.

This means the correlation pattern is rotated one cycle in only a 37-μs period of integration. The fringe rotation continuously changes the phase, but the K-3 correlation processor uses three-level approximation

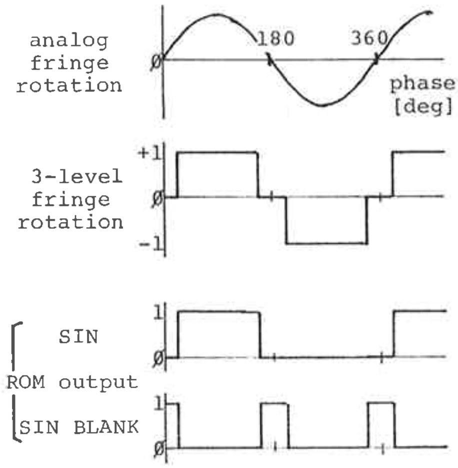


Fig. 5 Fringe phase compensation.

to simplify the hardware shown in Fig. 5. The fringe rotation can be compensated for up to 31 kHz.

5) Compensation of the fringe acceleration

The maximum rate of the fringe rotation, called fringe acceleration, is 0.98 Hz/sec(1). This should be also compensated for, because the phase is rotated one cycle per second. The fringe rotator of the K-3 correlation processor can set the fringe phase rate up to 931 Hz/sec, which covers the maximum fringe rate.

The rate of the fringe acceleration, which is 0.167 mHz/sec/sec, can be ignored for an 8-second integration period.

6) Fractional bit compensation

The fringe phase should be compensated for on the frequency, because it differs with the observed frequency. The K-3 correlation processor compensates for the fringe phase on the center frequency of the receiving band in the time domain, so that the fringe phase is not perfectly compensated for on the other frequency. The phase not compensated for is called a "fractional bit".

In order to reduce the fractional bit, the K-3 correlation processor makes the fringe rotator phase jump 90 degrees at the same time of the one-bit shift. The coherence loss of this method is calculated as 4%(4).

7) Correlation and integration

The one-bit sampled data, which is used in the Mark III VLBI format, is simply correlated by the exclusive-or gate circuit. Each correlation unit of the K-3 correlation processor has eight bit lags. The lag number can be extended to 64 bit lags in one crate using the eight correlation units for one channel data which can be used for fringe search.

8) Detection of the delay calibration signal

In order to compensate for the phase difference among the observation channels for the bandwidth synthesis, a comb signal is added at the RF. The K-3 correlation processor correlates the observed data and the two-level tone signal, which is generated in the delay calibration detector. This is similarly to the correlation processing.

9) Pulsar gate

The K-3 correlation processor also has the gate function for pulsar observation. When it receives a pulsar gate command from the host computer, the correlation is done only during the period of the gate in order to increase the S/N.

10) Calculation of the data time difference

The host computer needs to know the observed time difference between the data stream of the two stations in order to control the speed of the data recorder, which is necessary for maintaining synchronization. The observed data time difference from a priori is called a "synchronization error". This error is calculated in the K-3 correlation processor using the time code data and the value of the bit counter, which are obtained by the decoders X and Y.

4. Development Plan of the K-4 Correlation Processor

The K-4 VLBI system is being developed by the CRL. The analog equipment, such as the local oscillator, the IF distributor and the video converter, and the data recorder have already been developed(1)(5). This equipment is currently being used for the domestic VLBI experiments. It is now commercially available by Japanese manufacturing companies.

The K-4 system will be completed when the K-4 correlation processor is developed.

Some specifications of the K-4 correlation processor compared with the K-3 correlation processor are shown in Table 2. The main features of the K-4 correlation processor are:

(1) Based on the standard geodetic VLBI experiments using bandwidth synthesis technology

The K-4 correlation processor is based on 16-channel bandwidth synthesis observations in order to cover the 14-channel observation mode which is commonly used for conventional geodetic VLBI experiments.

(2) Fully compatible with K-4 data recorder

The K-4 data recorder performs complete synchronization, so that a synchronization function is not needed in a correlation processor. This simplify hardware of a correlation processor.

(3) Compact

Because of improved logic circuit technology, the K-4 correlation processor can be designed more compactly than the K-3. This allows easier relocation.

(4) High processing speed

The K-3 correlation processor runs at up to 8 Mbps, which is twice as fast as the usual observation rate of 4 Mbps. A computer should control the speed of the data recorders in order to synchronize the output data when the K-3 data recorder is used. It takes not short time to synchronize the data compared with the correlation time.

The K-4 data recorder has full synchronization capabilities built into it. Thus, the tape synchronization time is shorter than that of the K-3 data recorder and no computer control is needed. The K-4 correlation processor is designed to run at 16 Mbps, which reduces the total data processing time.

(5) Processing capability of millisecond pulsar signals

Millisecond pulsars were discovered few years ago, and the interval of the pulse radiated from some of them is expected to be more stable than the cesium frequency standard in long term. CRL has been developing a timing measurement system for these pulsars(7), and pulsar VLBI is also needed for radio astrometry.

Radio signals from the millisecond pulsars are weak compared with those of quasars observed by the geodetic VLBI experiments. Therefore, the gate function is needed for correlation processing in order to increase correlation amplitude. The pulsar gate of the K-4 correlation processor is designed to gate every bit unit, while the K-3 correlation processor can gate only once a parameter period, or a 5 milliseconds,

Table 2 Comparison between the VLBI correlation processors

	K-3	K-4
year completed	1984	1992
data input	K-3/Mark III	K-4
number of lags	8	>64
speed at 16 ch	8 Mbps	16 Mbps
sample bit	1	1/2/3/4/8/
max. fringe rate	32 kHz	>4 MHz
phase resolution	28 bits	32 bits
common mode	no	yes
phase cal. detect	1.25–160 kHz	not fixed
accumulate counter	24 bits	23 bits
parameter period	5 ms–8 s	5 ms–4 s
pulsar gate	once/pp	unit of one sample
main logic	MSI	FPGA

while a pulse period of a pulsar 1937+21 is 1.6 milliseconds.

(6) Flexible functions using FPGA (field programmable gate array)

FPGA is adopted in the K-4 correlation processor. It consists of several thousand logic gates and the internal circuit can be changed by personal computer. FPGA allows the correlation processor to flexibly process different kinds of observed data with one hardware.

(7) Multibit sampled data processing available for radio astronomy

One or two channels of the K-4 correlation processor can process the multibit sampled data, which is needed for the radio astronomy. Correlation processing of dual-bit sampled data increases correlation amplitude for a short observation time, which is especially useful for mobile VLBI stations with a small antenna and crystal-cesium frequency standard.

(8) High fringe stopping for higher frequency observation or for space VLBI

Higher frequency VLBI experiments, such as 22 GHz or 43 GHz, have begun for highly accurate geodesy with a wider bandwidth. In space VLBI, the baseline length is much longer than the earth surface experiment. Both result in a higher fringe rotation rate. The K-4 correlation processor is designed to be able to stop this.

5. Conclusions

The K-3 correlation processor, which has various functions such as high-speed processing and long integration time, was developed by CRL. This processor has been the only VLBI correlation processor in Japan for more than five years. It is used for processing VLBI experiments involving the CDP, the Western Pacific VLBI Network, the first Antarctica, highly transportable VLBI station with a 3-m antenna and domestic experiments[6]. The K-3 correlation processor was developed with the K-3 data acquisition terminal.

The development of the K-4 correlation processor has been started by the Communications Research Laboratory. It is completely designed using the advanced functions of the K-4 data recorder, and is targeted as the next-generation processor.

Acknowledgement

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